Engineering Diagrams Set

HP 3000 Series III

(Products 32421A and 32435A)

19447 Pruneridge Ave., Cupertino, California 95014



NOTICE

The information contained in this document is subject to change without notice.

HEWLETT-PACKARD MAKES NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Hewlett-Packard shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance or use of this material.

This document contains proprietary information which is protected by copyright. All rights are reserved. No part of this document may be photocopied or reproduced without the prior written consent of Hewlett-Packard Company.

LIST OF EFFECTIVE PAGES

The list of effective pages gives the most recent date on which the technical material on any given page was altered. If a page is simply rearranged because of a technical change on a previous page, it is not listed as a changed page. Within the manual, changes are marked with a vertical bar in the margin.

A11	pages	original	issueAPRIL	1980
***	pasco	01 1811141		100

PRINTING HISTORY

New editions incorporate all update material since the previous edition. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The date on the title page changes only when a new edition is published. If minor corrections and updates are incorporated, then the manual is reprinted but neither the date on the title page nor the edition change.

First Printing......APRIL 1980

GENERAL INFORMATION

This Engineering Diagrams Set provides schematics, component layouts, and signal and power distribution diagrams for the HP 3000 Series III Computer Systems.

Products 32421A and 32435A are included. Many of the diagrams are common to both. THOSE UNIQUE TO ONE OF THE PRODUCTS ARE LABELED ACCORDINGLY.

The Set is divided into four sections. Section 1 contains rack diagrams and power and signal wiring information. Diagrams and tables unique to the 32421A appear first, followed by those for the 32435A; diagrams and tables common to both products appear last.

Section II contains the schematics and component location diagrams for the CPU and Memory Modules. They appear in numerical order.

Section III contains I/O PCA diagrams, in numerical order.

Section IV contains individual power supply diagrams. Those for the 32421A appear first, followed by those for the 32435A.

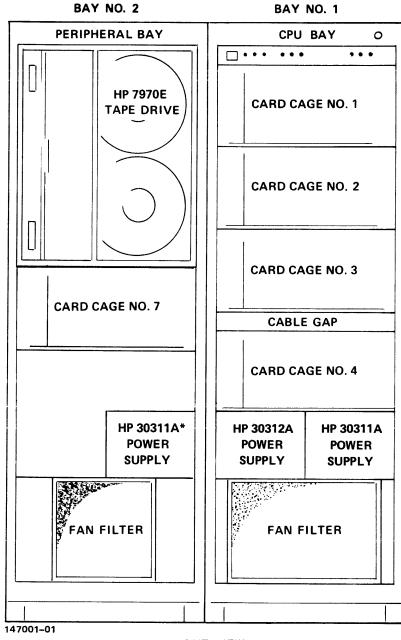
NOTE

On some diagrams, a box containing dates appears in the upper right corner. THOSE DATES SHOULD BE IGNORED. Each PCA was examined for changes shortly before this set was printed in April 1980.

SECTION I - RACK DIAGRAMS/POWER AND SIGNAL WIRING LAYOUTS

CONTENTS

FIGURE or TABLE NO.	DESCRIPTION	FIGURE or TABLE NO.	DESCRIPTION
Fig. 1-1	A21A Racking Plan 200, Racking Plan Slot Assignments Kit, Assignments 200, Assignments Kit, Assignments Cable Terminators Vitem Flat Cables Vitem Flat Cables Vitem Flat Cables Vitem Vite	Fig. 1-32	ion 200, Power Bus Connection lane Signal Distribution List er Bus (Non-Memory Card Cage)



FRONT VIEW
(DOORS OMITTED FOR CLARITY)

* Optionally installed at the factory or field installed using the HP 30418A Upgrade Kit for 768K-word or 1024K-word memory.

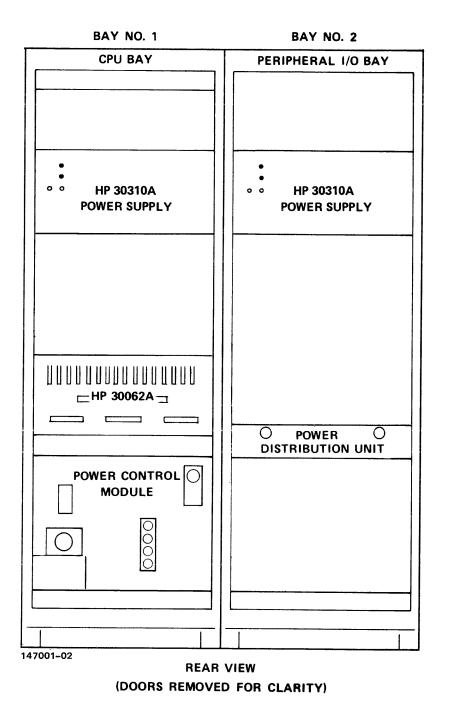
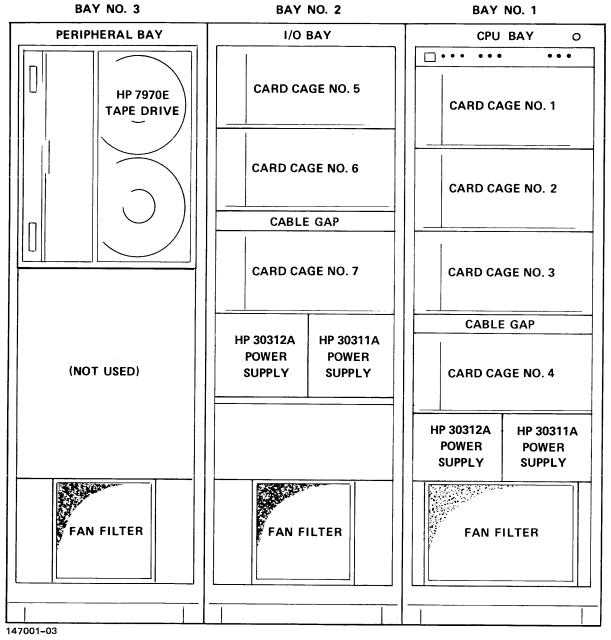
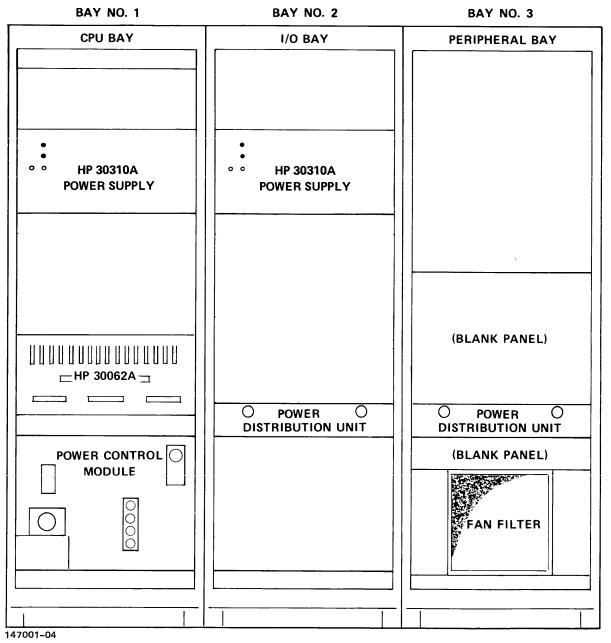


Figure 1-1. HP 3000 Series III (32421A) Racking Plan, Front and Rear Views



FRONT VIEW (DOORS OMITTED FOR CLARITY)



REAR VIEW (DOORS REMOVED FOR CLARITY)

Figure 1-2. HP 3000 Series III (32421A), Option 200, Racking Plan, Front and Rear Views

Table 1-1. PCA Slot Assignments (32421A)

SLOT

A2 A3

CARD CAGE

		SLOT	PRINTED CIRCUIT ASSEMBLY
	CARD CAGE NO.1	A1 A2 A3 A4 A5 A6 A7 A8 A9	Reserved for maintenance panel PCA, 30012-60001 Extended Instruction Set 30003-60021 Read Only Memory 30003-60022 Skip and Special Field 30003-60003 Arithmetic and Logic Unit 30003-60004 R Bus 30003-60005 S Bus 30003-60006 Current Instruction Register 30003-60007 Module Control Unit 30003-60028 Input Output Processor
	CARD CAGE NO.2	A1 A2 A3 A4 A5 A6 A7 A8 A9	30032-60001 Terminal Data Interface 30061-60001 Terminal Control Interface Reserved for 204 Modem capability 30009-60002 Fault Logging Interface 30008-60003 Memory Array (128K) Available to add 128K Available to add 128K Available to add 128K 30007-60005 Memory Control and Logging
PRINTED CIRCUIT ASSEMBLY Available for programmed (SIO) or direct I/O 30215-60002 Magnetic Tape Controller Processor 30215-60006 Magnetic Tape Controller	CARD CAGE NO.3	A1 A2 A3 A4 A5 A6 A7 A8 A9	Available for add-on memory 30030-60020 Selector Channel Port Controller 30030-60021 Selector Channel Register 30030-60003 Selector Channel Control 30030-60011 Selector Channel Sequencer
Available for programmed (SIO) or direct I/O	CARD CAGE NO.4	A1 A2 A3 A4 A5 A6 A7 A8 A9	30036-60002 Multiplexer Channel Available for programmed (SIO) or direct I/O. Available for programmed (SIO) or direct I/O. Available for programmed (SIO) or direct I/O. 30031-60001 System Clock Interrupt Poll Jumper (IPJ) 30000-60001 30229-60001 7905A/20A/25A Interface 13037-60028 Disc Controller 13037-60024 Error Correction 13037-60001 Microprocessor

Table 1-2. PCA Slot Assignments (32421A) with HP 30418A Upgrade Kit Installed

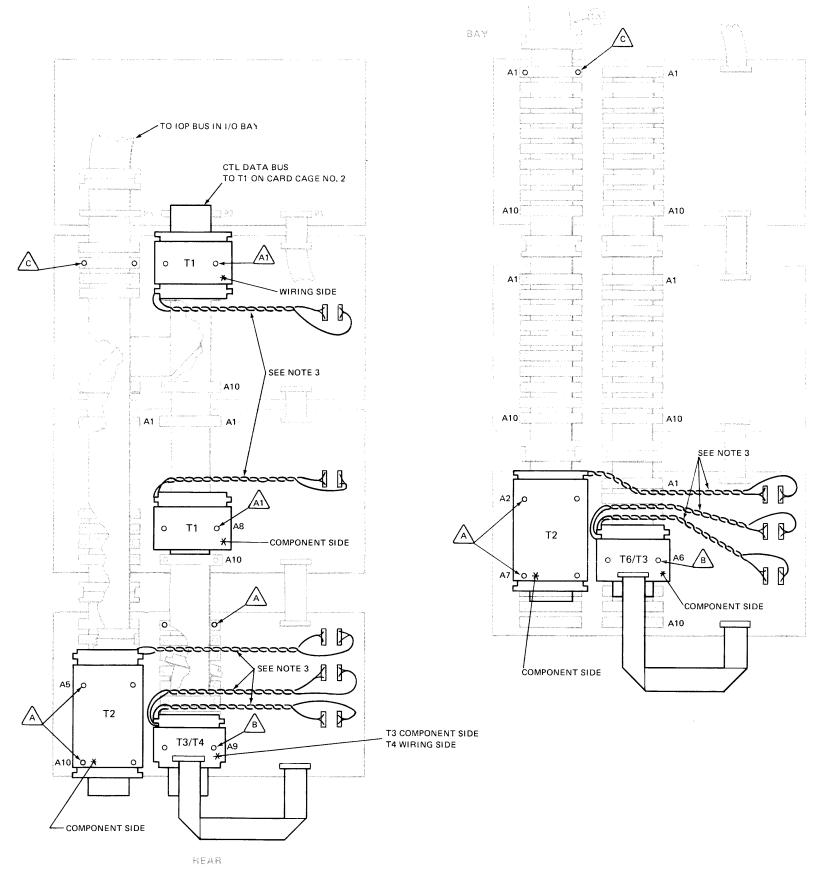
				SLOT	PRINTED CIRCUIT ASSEMBLY
			CARD CAGE NO.1	A1 A2 A3 A4 A5 A6 A7 A8 A9 A10	Reserved for maintenance panel PCA. 30012-60001 Extended Instruction Set 30003-60021 Read Only Memory 30003-60022 Skip and Special Field 30003-60003 Arithmetic and Logic Unit 30003-60004 R Bus 30003-60005 S Bus 30003-60006 Current Instruction Register 30003-60007 Module Control Unit 30003-60028 Input Output Processor
			CARD CAGE NO.2	A1 A2 A3 A4 A5 A6 A7 A8 A9 A10	30032-60001 Terminal Data Interface 30061-60001 Terminal Control Interface Reserved for 203 Modem capability 30009-60002 Fault Logging Interface 30008-60003 Memory Array (128K) 30008-60003 Memory Array (128K) 30008-60003 Memory Array (128K) 30008-60003 Memory Array (128K) 30007-60005 Memory Control and Logging
ſ	SLOT	PRINTED CIRCUIT ASSEMBLY	CARD CAGE NO.3	A1 A2 A3 A4 A5 A6	30007-60004 Memory Control and Logging Slots A2 and A3 are available to add 256K 30008-60003 Memory Array (128K) 30008-60003 Memory Array (128K)
	A1 A2 A3	Available for programmed (SIO) or direct I/O 30215-60002 Magnetic Tape Controller Processor 30215-60006 Magnetic Tape Controller	NU.3	A7 A8 A9 A10	30030-60020 Selector Channel Port Controller 30030-60021 Selector Channel Register 30030-60003 Selector Channel Control 30030-60011 Selector Channel Sequencer
CARD CAGE NO.7	A4 A5 A6 A7 A8 A9 A10	Available for programmed (SIO) or direct I/O	CARD CAGE NO.4	A1 A2 A3 A4 A5 A6 A7	30036-60002 Multiplexer Channel Available for programmed (SIO) or direct I/O. Available for programmed (SIO) or direct I/O. Available for programmed (SIO) or direct I/O. 30031-60001 System Clock Interrupt Poll Jumper (IPJ) 30000-60001 30229-60001 7905A/20A/25A Interface 13037-60028 Disc Controller
				A9 A10	13037-60024 Error Correction 13037-60001 Microprocessor

Table 1-3. PCA Slot Assignments (32421A), Option 200

	SLOT	PRINTED CIRCUIT ASSEMBLY		SLOT	PRINTED CIRCUIT ASSEMBLY
	A1	30036-60002 Multiplexer Channel		A1	Reserved for maintenance panel PCA.
•	A2	30215-60002 Magnetic Tape Controller Processor		A2	30012-60001 Extended Instruction Set
	А3	30215-60006 Magnetic Tape Controller		А3	30003-60021 Read Only Memory
	A4	30031-60001 System Clock		A4	30003-60022 Skip and Special Field
CARD	A5	Available for programmed (SIO) or direct I/O	CARD	A5	30003-60003 Arithmetic and Logic Unit
CAGE	A6	Available for programmed (SIO) or direct I/O	CAGE	A6	30003-60004 R Bus
NO.5	A7	Available for programmed (SIO) or direct I/O	NO.1	A7	30003-60025 S Bus
	A8	Available for programmed (SIO) or direct I/O		A8	30003-60006 Current Instruction Register
	A9	Available for programmed (SIO) or direct I/O		A9	30003-60007 Module Control Unit
	A10	Available for programmed (SIO) or direct I/O		A10	30003-60028 Input Output Processor
	A1	Available for programmed (SIO) or direct I/O		A1	30032-60001 Terminal Data Interface
	A2	Available for programmed (SIO) or direct I/O		A2	30061-60001 Terminal Control Interface
	A3	Available for programmed (SIO) or direct I/O		A3	Reserved for 203 Modem capability
	A4	Available for programmed (SIO) or direct I/O		A4	30009-60002 Fault Logging Interface
CARD	A5	Available for programmed (SIO) or direct I/O	CARD	A5	
CAGE	A6	Available for programmed (SIO) or direct I/O	CAGE	A6	30008-60003 Memory Array (128K)
NO.6	A7	Available for programmed (SIO) or direct I/O	NO.2	A7	Available to add 128K.
	A8	Available for programmed (SIO) or direct I/O		A8	Available to add 128K.
	A9	Available for programmed (SIO) or direct I/O		A9	Available to add 128K.
	A10	Available for programmed (SIO) or direct I/O		A10	30007-60005 Memory Control and Logging
	A1	Available for programmed (SIO) or direct I/O		A1	Available for add-on memory
	A2	Available for programmed (SIO) or direct I/O		A2	Available for add-on memory
	A3	Available for programmed (SIO) or direct I/O		A3	Available for add-on memory
	Α4	Available for programmed (SIO) or direct I/O		A4	Available for add-on memory
CARD	A5	Available for programmed (SIO) or direct I/O	CARD	A5	Available for add-on memory
CAGE	A6	Available for programmed (SIO) or direct I/O	CAGE	A6	
NO.7	A7	Available for programmed (SIO) or direct I/O	NO.3	A7	30030-60020 Selector Channel Port Controller
	A8	Reserved for second disc controller		A8	30030-60021 Selector Channel Register
	A9	Reserved for second disc controller	Ì	A9	30030-60003 Selector Channel Control
	A10	Reserved for second disc controller		A10	30030-60011 Selector Channel Sequencer
-				A1	Reserved for second Selector Channel
				A2	Reserved for second Selector Channel
				A3	Reserved for second Selector Channel
				A4	IJP 30000-60001
			CARD	A5	Reserved for second 7905A/20A/25A Interface
			CAGE	A6	IJP 30000-60001
			NO.4	A7	30229-60001 7905A/20A/25A Interface
				A8	13037-60028 Disc Controller
				A9	13037-60024 Error Correction
				A10	13037-60001 Microprocessor
				1	, ,

Table 1-4. PCA Slot Assignments (32421A), Option 200, with HP 30418A Upgrade Kit Installed

ı			1 1		
	SLOT	PRINTED CIRCUIT ASSEMBLY		SLOT	PRINTED CIRCUIT ASSEMBLY
CARD CAGE NO.5	A1 A2 A3 A4 A5 A6 A7 A8 A9 A10	30036-60002 Multiplexer Channel 30215-60002 Magnetic Tape Controller Processor 30215-60006 Magnetic Tape Controller 30031-60001 System Clock Available for programmed (SIO) or direct I/O	CARD CAGE NO.1	A1 A2 A3 A4 A5 A6 A7 A8 A9	Reserved for maintenance panel PCA. 30012-60001 Extended Instruction Set 30003-60021 Read Only Memory 30003-60022 Skip and Special Field 30003-60003 Arithmetic and Logic Unit 30003-60004 R Bus 30003-60005 S Bus 30003-60006 Current Instruction Register 30003-60007 Module Control Unit 30003-60028 Input Output Processor
CARD CAGE NO.6	A1 A2 A3 A4 A5 A6 A7 A8 A9	Available for programmed (SIO) or direct I/O	CARD CAGE NO.2	A1 A2 A3 A4 A5 A6 A7 A8 A9	30032-60001 Terminal Data Interface 30061-60001 Terminal Control Interface Reserved for 203 Modem capability 30009-60002 Fault Logging Interface 30008-60003 Memory Array (128K) 30007-60005 Memory Control and Logging
CARD CAGE NO.7	A1 A2 A3 A4 A5 A6 A7 A8 A9	Available for programmed (SIO) or direct I/O Reserved for second disc controller Reserved for second disc controller Reserved for second disc controller	CARD CAGE NO.3	A1 A2 A3 A4 A5 A6 A7 A8 A9	30007-60005 Memory Control and Logging Available to add 128K Available to add 128K 30008-60003 Memory Array (128K) 30008-60003 Memory Array (128K) 30030-60020 Selector Channel Port Controller 30030-60021 Selector Channel Register 30030-60003 Selector Channel Control 30030-60011 Selector Channel Sequencer
			CARD CAGE NO.4	A1 A2 A3 A4 A5 A6 A7 A8 A9	Reserved for second Selector Channel Reserved for second Selector Channel Reserved for second Selector Channel IJP 30000-60001 Reserved for second 7905A/20A/25A Interface IJP 30000-60001 30229-60001 7905A/20A/25A Interface 13037-60028 Disc Controller 13037-60024 Error Correction 13037-60001 Microprocessor



NOTES:

1. TERMINATORS ARE IDENTIFIED AS FOLLOWS:

TERMINATOR	QUANTITY	PART NUMBER
T1	2	30003-60030
T2	2	30001-60016
T3	2	30001-60021
T4	1 *	30030-60015
T6	1	30035-60003

- PRINTED CIRCUIT EDGE CONNECTOR J1 OF A TERMI-NATOR PLUGS INTO A FLAT CABLE CONNECTOR TO TERMINATE THE CABLE RUN. CORRECT TERMINATOR ORIENTATION IS ASSURED IF YOU KEEP PINS 49 AND 50 OF THE EDGE CONNECTOR TO THE LEFT WHEN TER-MINATING THE FLAT CABLE.
- 3. EACH TERMINATOR HAS A RED TWISTED PAIR CABLE WHICH CONNECTS FROM EDGE P1 OF THE TERMINATOR PCA TO PINS 2 AND 1 (+5 VOLTS) ON ANY POWER BUS CONNECTOR P1. A BLACK TWISTED PAIR CABLE CONNECTS FROM THE PCA TO PINS 16 AND 15 OF THE SAME POWER BUS CONNECTOR.
- 4. T1/T4 = T1 IS BENEATH; T4 IS VISIBLE. T6/T3 = T6 IS BENEATH; T3 IS VISIBLE.

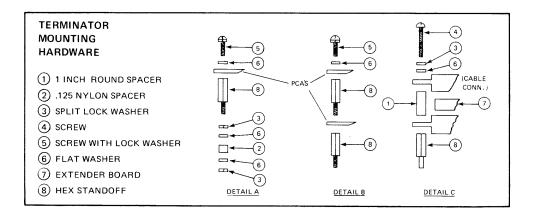


A1 = DETAIL A, ITEMS 2, 3, 5, 6, 8

B = DETAIL B

C = DETAIL C

= FLAT CABLE CONNECTORS JOINED WITH EXTENDER BOARDS



047001--05

Figure 1-3. Flat Cable Terminators (32421A)

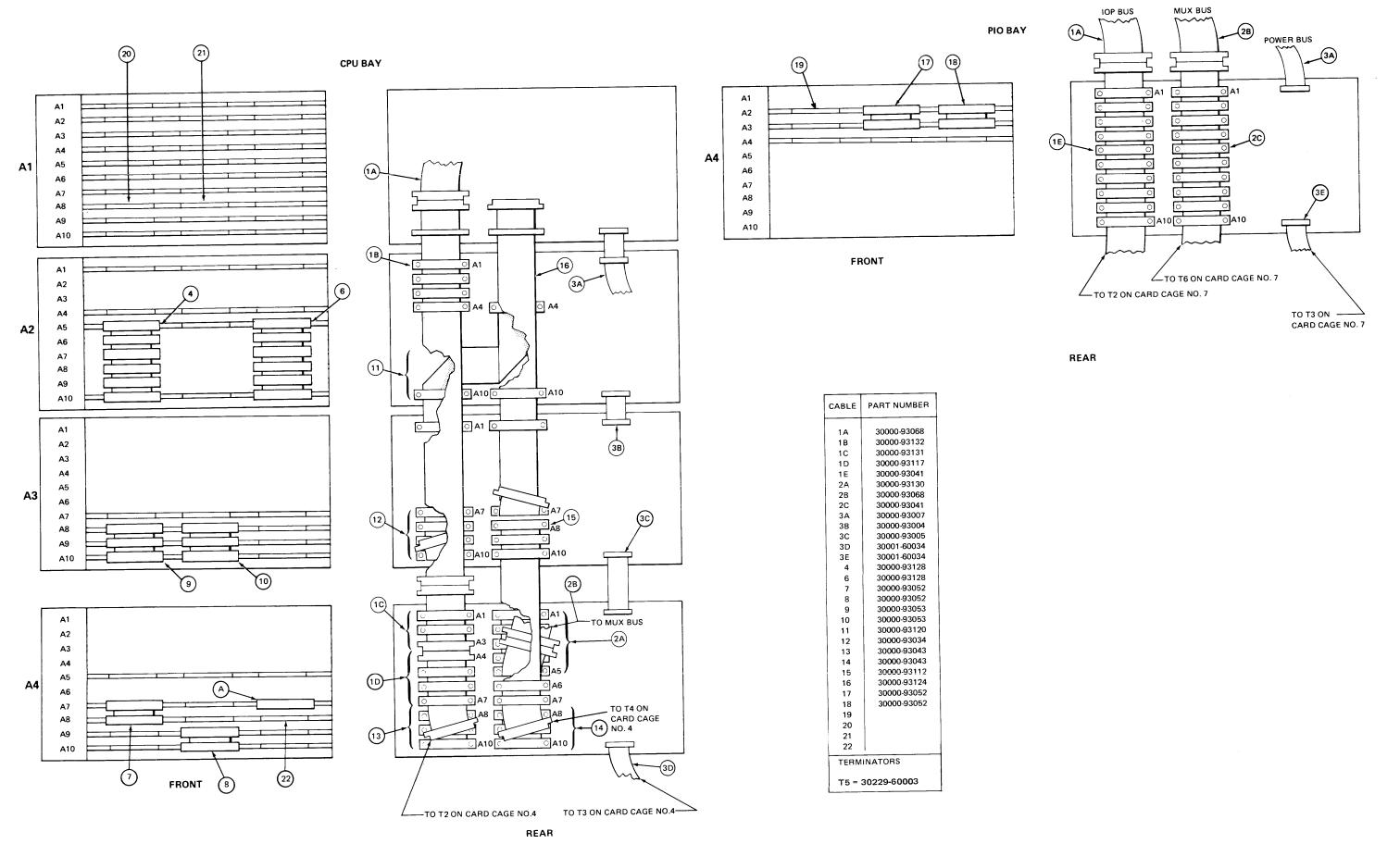
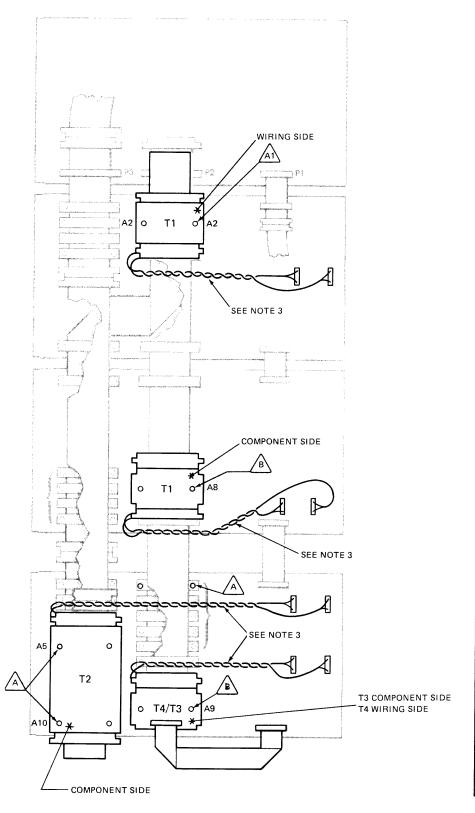
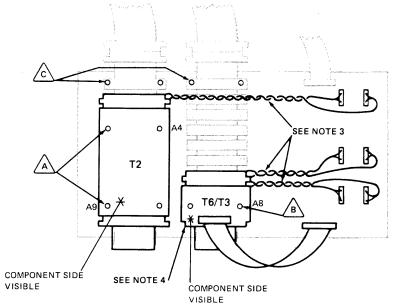


Figure 1-4. System Flat Cables (32421A)





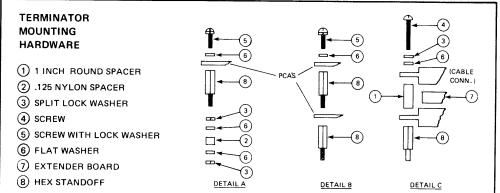
A = DETAIL A, ITEMS 5, 6, 8

DETAIL A, ITEMS 2, 3, 5, 6, 8

B = DETAIL B

C = DETAIL C

= FLAT CABLE CONNECTORS JOINED WITH EXTENDER BOARDS



047001-07

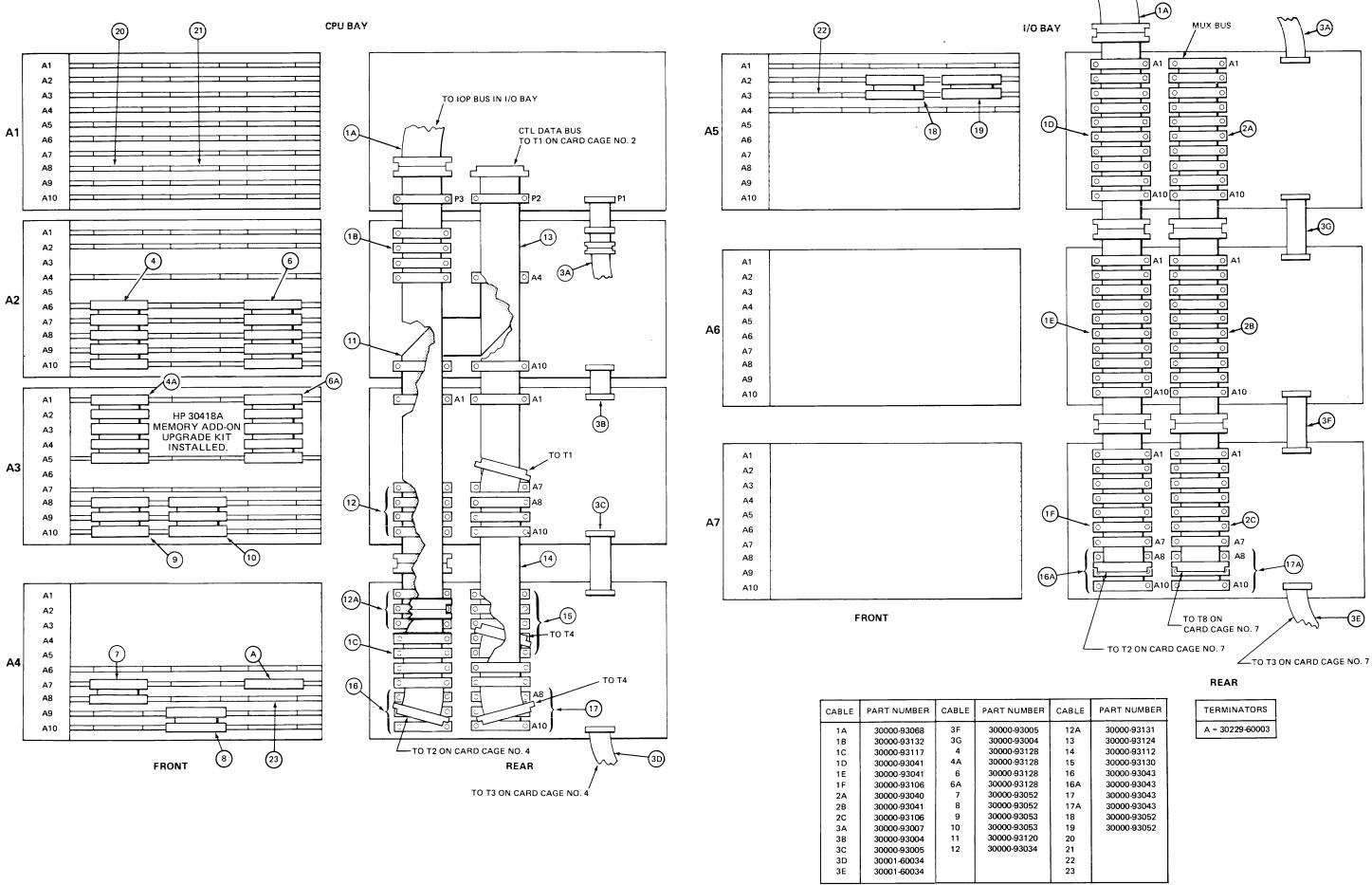
NOTES:

1. TERMINATORS ARE IDENTIFIED AS FOLLOWS:

ERMINATOR	QUANTITY	PART NUMBER
T1	2	30003-60030
T2	2	30001-60016
T3	2	30001-60021
T4	1 *	30030-60015
T6	1	30035-60003

- 2. PRINTED CIRCUIT EDGE CONNECTOR J1 OF A TERMINATOR PLUGS INTO A FLAT CABLE CONNECTOR TO TERMINATE THE CABLE RUN. CORRECT TERMINATOR ORIENTATION IS ASSURED IF YOU KEEP PINS 49 AND 50 OF THE EDGE CONNECTOR TO THE LEFT WHEN TERMINATING THE FLAT CABLE.
- 3. EACH TERMINATOR (EXCEPT T5) HAS A RED TWISTED PAIR CABLE WHICH CONNECTS FROM EDGE P1 OF THE TERMINATOR PCA TO PINS 2 AND 1 (+5 VOLTS) ON ANY POWER BUS CONNECTOR P1. A BLACK TWISTED PAIR CABLE CONNECTS FROM THE PCA TO PINS 16 AND 15 OF THE SAME POWER BUS CONNECTOR.
- 4. T3/T4 = T1 IS BENEATH; T4 IS VISIBLE. T6/T3 = T6 IS BENEATH; T3 IS VISIBLE.

Figure 1-5. Flat Cable Terminators (32421A), with Option 200



147001-08

Figure 1-6. System Flat Cables (32421A), with Option 200

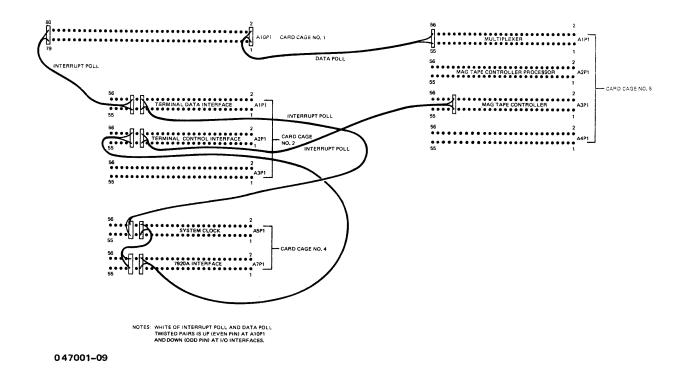


Figure 1-7. Typical Interrupt Poll Cabling (32421A)

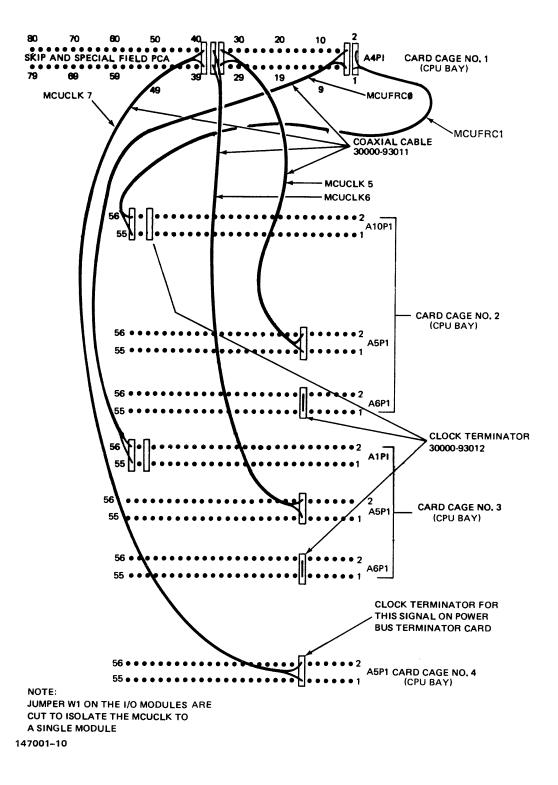


Figure 1-8. CPU Bay Clock Jumpers and Terminators (32421A)

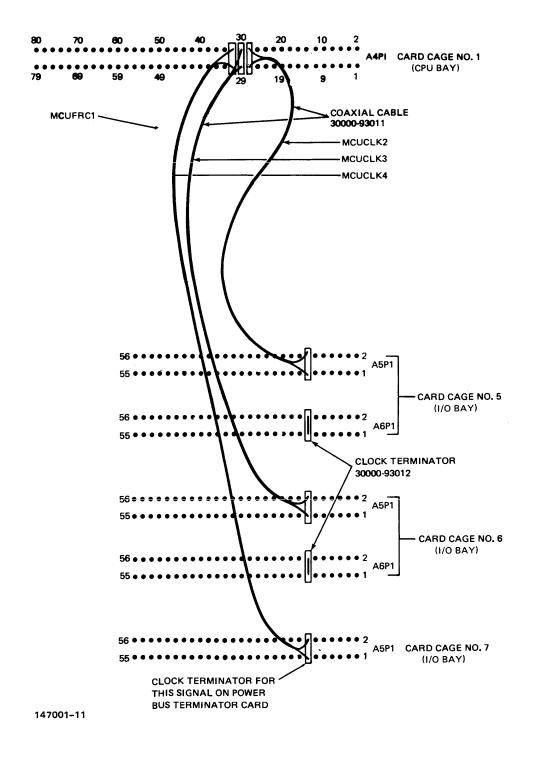


Figure 1-9. I/O Bay Clock Jumpers and Terminators (32421A)

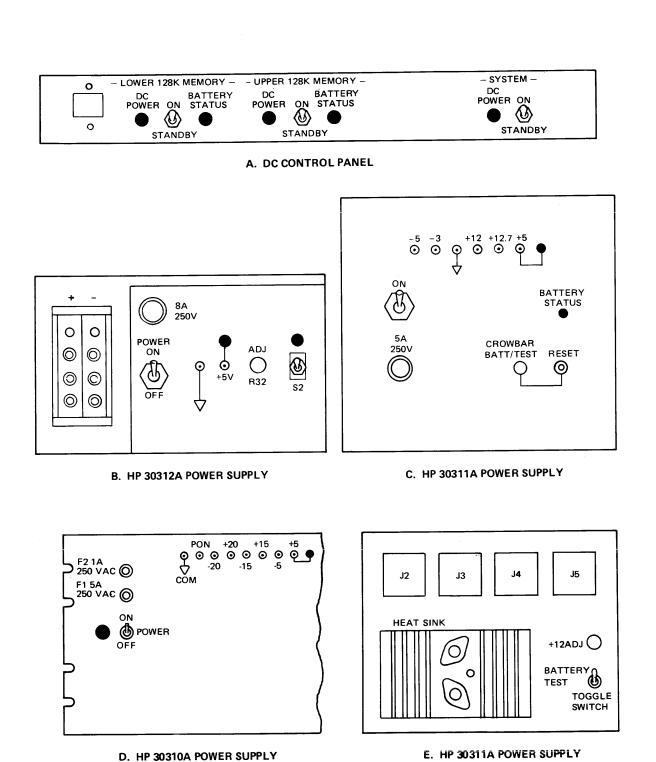


Figure 1-10. Power Controls and Indicators (32421A)

= TEST POINT
= INDICATOR

147001-12

(REAR VIEW)

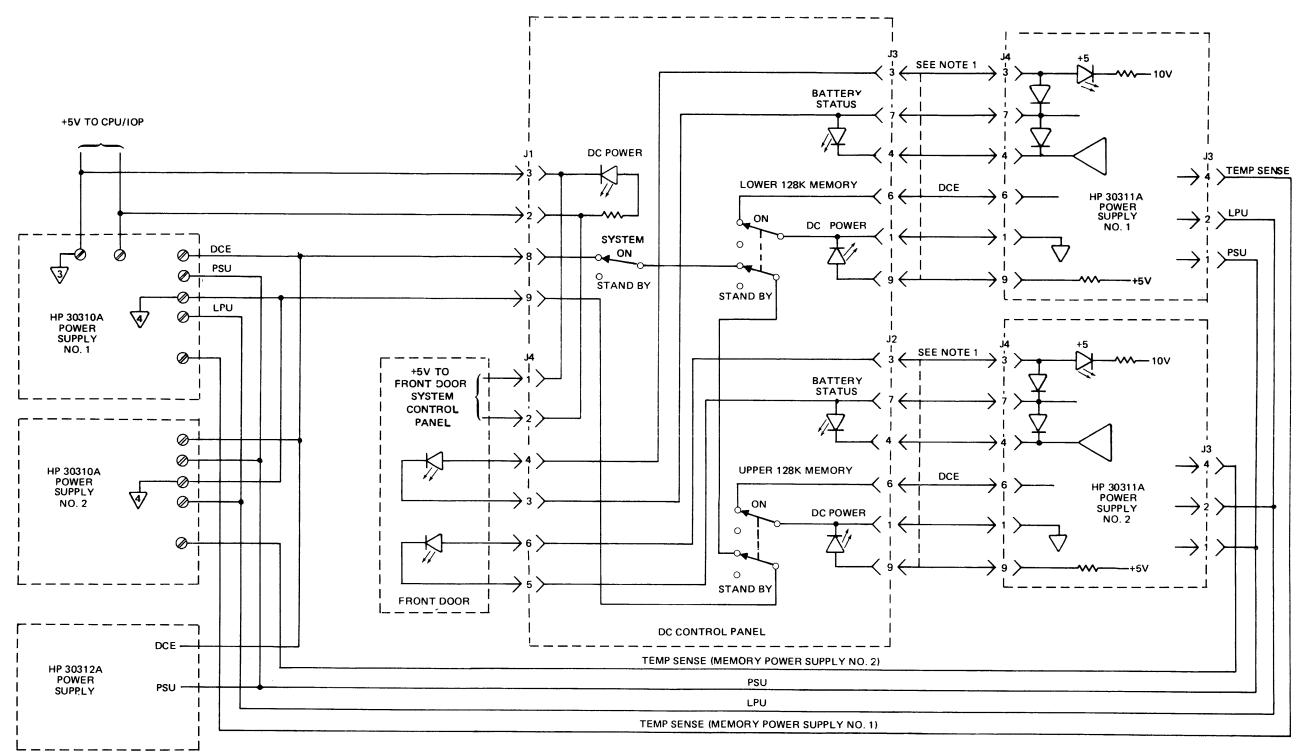
Table 1-5. Power Control and Indicator Functions (32421A)

DC Control Panel	Function
SYSTEM ON/STANDBY toggle switch.	In the ON position, enables DC voltage outputs of the HP 30310A and 30312A Power Supplies. In STANDBY, all DC power supply outputs are disabled. Batteries are then sustaining memory.
SYSTEM DC POWER indicator	Implies that system DC power is on by using +5 volts from the HP 30310A Power Supply to light its LED.
UPPER 128K MEMORY ON/STANDBY 2-pole toggle switch	In the ON position, one pole generates a DC Enable signal to its HP 30311A Power Supply. If the power supply is turned on, and if the SYSTEM ON/STANDBY and LOWER 128K MEMORY ON/STANDBY switches are ON, the power supply will power memory and maintain the charge on its battery. If either or both of these other switches are set to STANDBY, the HP 30311A powers memory by its battery backup power to the memory "refresh" circuits. The second pole maintains continuity of the system DC Enable line which enables the HP 30310A and HP 30312A Power Supply outputs. In the STANDBY position, the system DC Enable line is opened and all DC power supply outputs, except battery backuppower to the lower 128K of memory, are disabled.
UPPER 128K MEMORY DC POWER indicator	Indicates that upper memory power is on by using +5 volts from HP 30311A Power Supply No. 2 to light this LED.
UPPER 128K MEMORY BATTERY STATUS indicator	Indicates battery status of HP 30311A Power Supply No. 2 by being on, flashing, or off.
LOWER 128K MEMORY ON/STANDBY toggle switch	In the ON position, one pole generates a DC Enable signal to its HP 30311A Power Supply. If the power supply is turned on, and if the SYSTEM ON/STANDBY and UPPER 128K MEMORY ON/STANDBY switches on ON, the power supply will power memory and maintain the charge on its battery. If either or both of these other switches are set to STANDBY, the HP 30311A powers memory by its battery backup power to the memory "refresh" circuits. The second pole maintains continuity of the system DC Enable line which enables the HP 30310A and HP 30312A Power Supply

	outputs. In the STANDBY position, the system DC Enable line is opened and all DC power supply outputs, except battery backuppower to the upper 128K of memory are disabled.
LOWER 128K MEMORY DC POWER indicator	Indicates that lower memory power is on by using +5 volts from HP 30311A Power Supply No. 1 to light this LED.
LOWER 128K MEMORY BATTERY STATUS indicator	Indicates battery status of HP 30311A Power Supply No. 1 by being on, flashing or off.
HP 30310A Power Supply	Function
POWER ON/OFF toggle switch and indicator	Indicator lights when toggle switch is ON connecting AC power to power supply circuits. OFF position disables the HP HP 30310A.
HP 30311A Power Supply	Function
Power ON/OFF toggle switch	In ON position, connects "+20 volts" terminal from the HP 30310A Power Supply to the HP 30311A circuits to maintain the charge on the battery and to develop the required memory operating voltages. Off (down) position disables the HP 30311A and disconnects the battery to prevent discharging.
BATTERY TEST momentary toggle switch	Places power supply in a battery discharge mode for test purposes (simulates a power failure). Lights the battery test indicator.
RESET pushbutton	Resets the battery discharge mode return- ing the power supply to normal operation. Turns off the battery test indicator.
+5 indicator	When lighted, indicates that +5 volts is being produced by the HP 30311A Power Supply.

Table 1-5. Power Controls and Indicator Functions (32421A) (Cont.)

CROWBAR/BATT TEST indicator	Used in conjunction with the BATTERY STATUS indicator to determine if the crowbar circuit has fired and shut down the power supply.
BATTERY STATUS indicator	Indicates battery condition by: a. Being on continuously for fully- charged condition. A bad (open) battery will also produce this condition. b. Flashing at 2 Hz when discharging c. Flashing at 0.5 Hz when charging d. Being off if battery is low or not installed.
HP 30312A Power Supply	Function
POWER ON/OFF toggle switch	The ON position connects AC power to the power supply circuits. The OFF position removes AC power.
ADJ R32 potentiometer, S2 momentary toggle switch, and LED	The potentiometer is adjusted while the toggle switch is pressed until the LED in the upper right of the front panel lights and just goes out. When the toggle switch is released, the threshold level is incremented by 10 amperes.



- NOTES:
 1. ONE 9-CONDUCTOR 30311-60007 CABLE PER 30311A SUPPLY. PINS 2-2, 5-5, AND 8-8 ARE SPARES.
- ANY ADDITIONAL HP 30311A POWER SUPPLIES INCLUDED IN THE SYSTEM HAVE CONTROL LINES (EXCEPT TEMP SENSE) PARALLELED.

147001-13

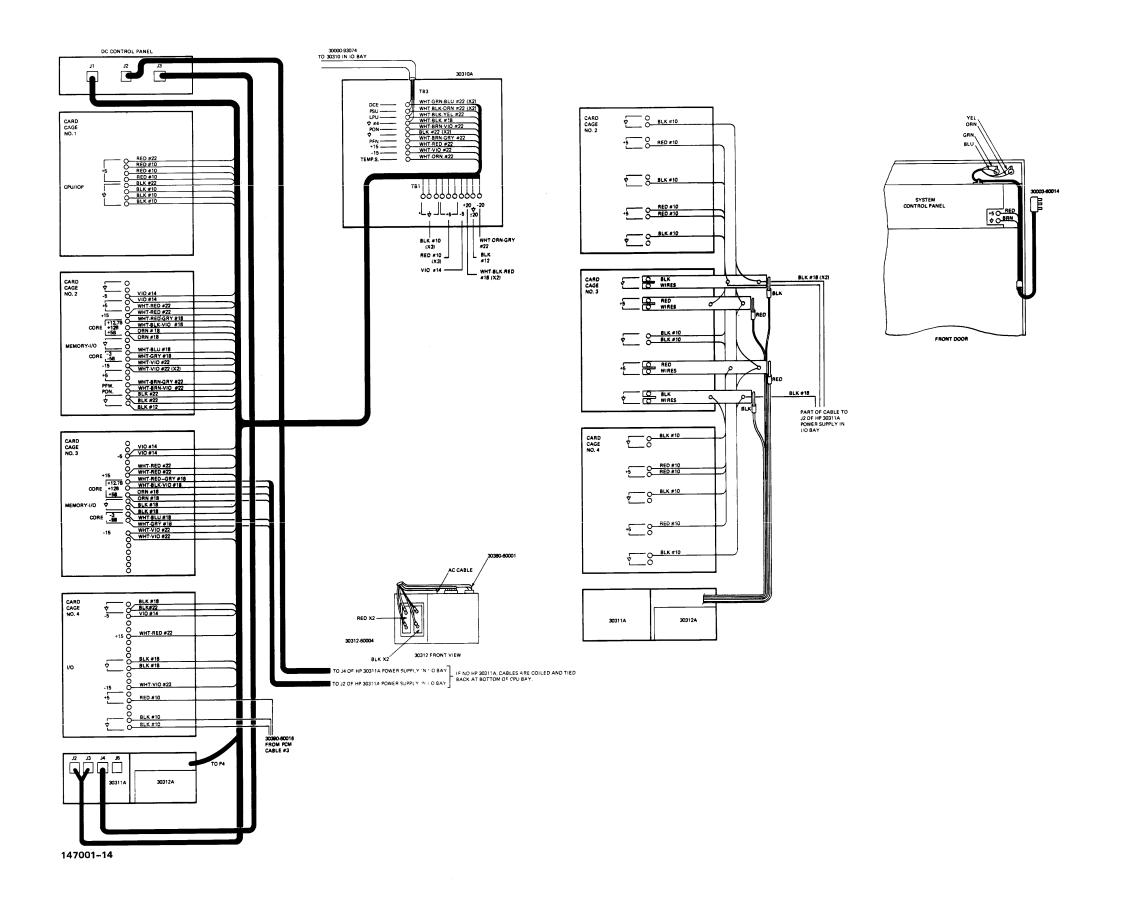
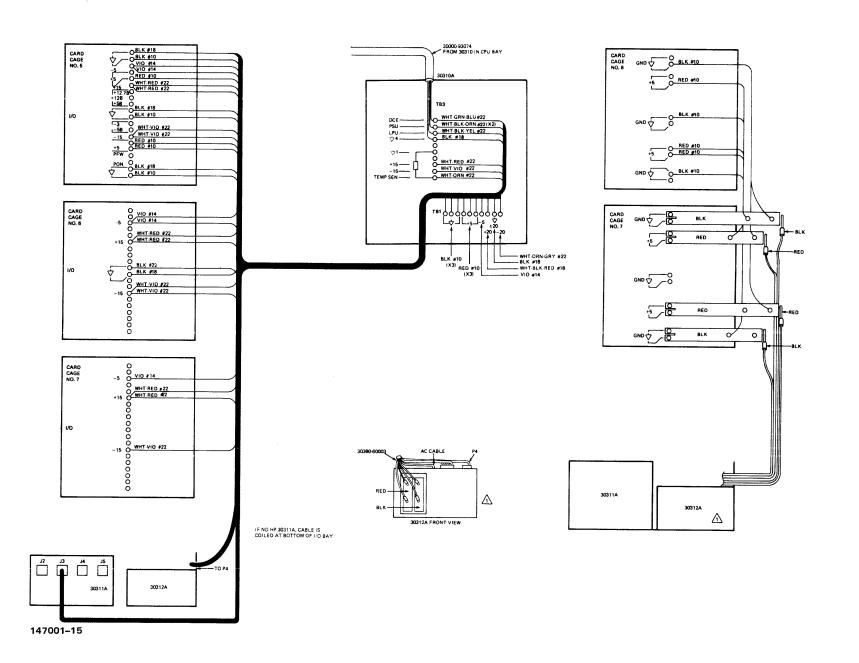


Figure 1-12. CPU Bay DC Wiring (32421A)



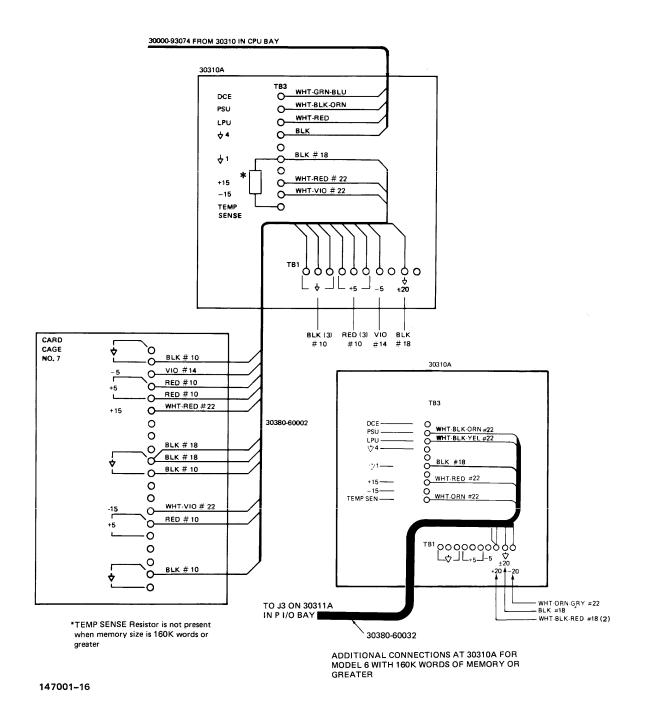


Figure 1-14. Peripheral and I/O Bay DC Wiring (32421A)

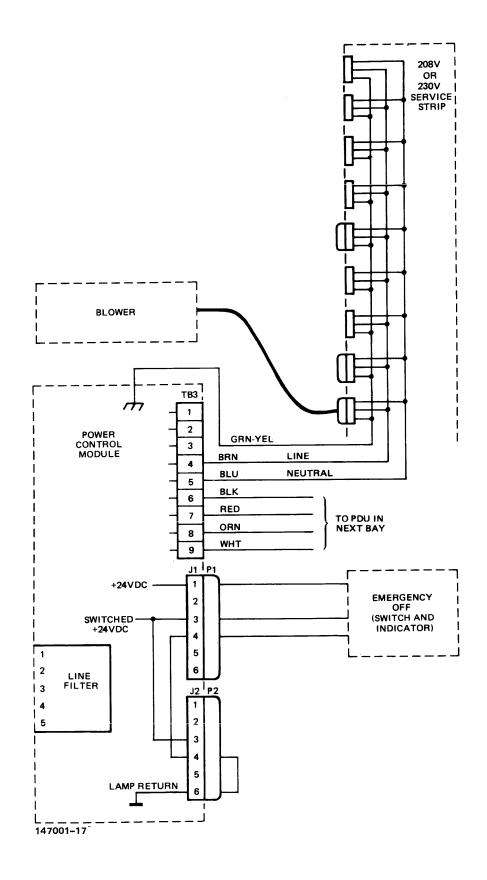


Figure 1-15. AC Distribution, CPU Bay (32421A)

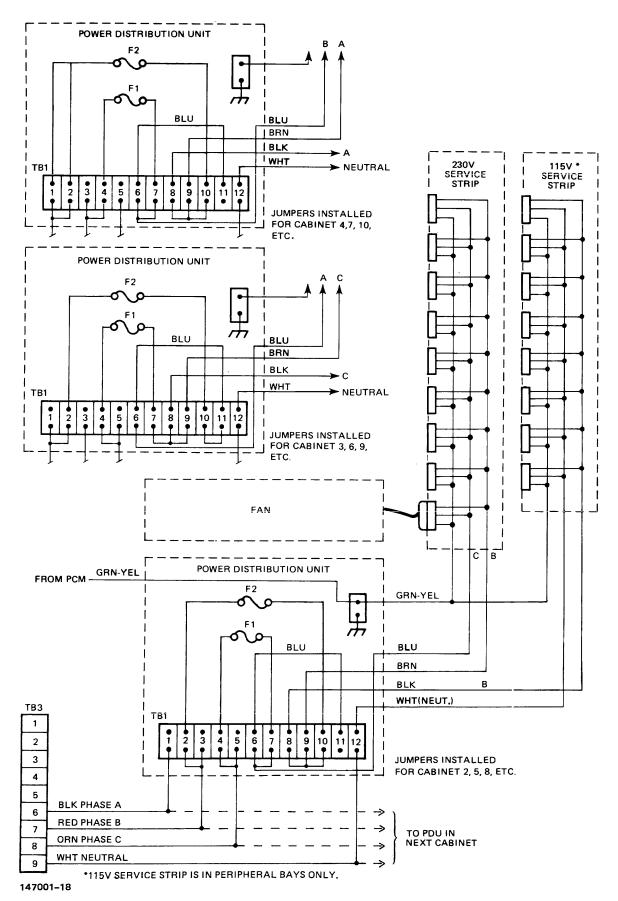


Figure 1-16. AC Distribution, Auxiliary Cabinets (120V/280V, 3Ph, 60 Hz) (32421A)

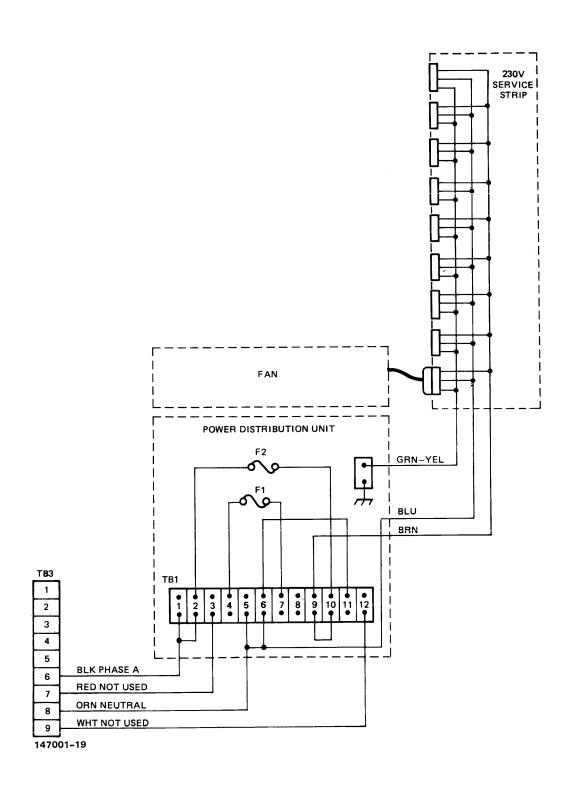
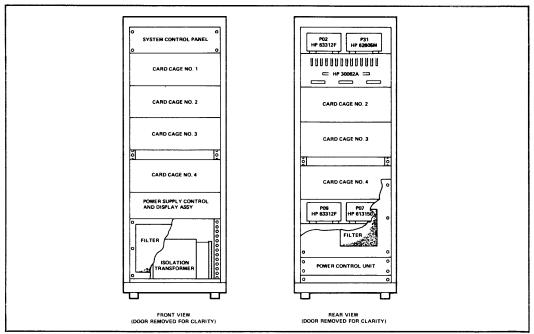
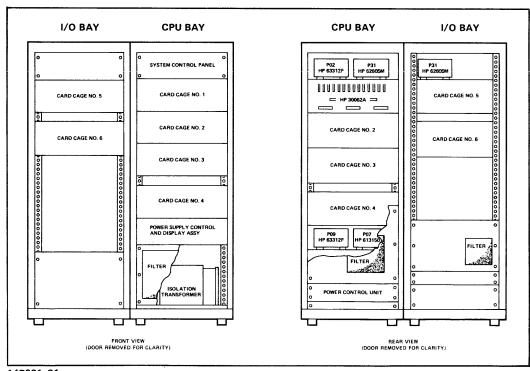


Figure 1-17. AC Distribution, Auxiliary Cabinets (230V, 1Ph, 50 Hz) (32421A)



147001-20

Figure 1-18. HP 3000 Series III Computer System (32435A)



147001-21

Figure 1-19. HP 3000 Series III Computer System (32435A) with Option 200

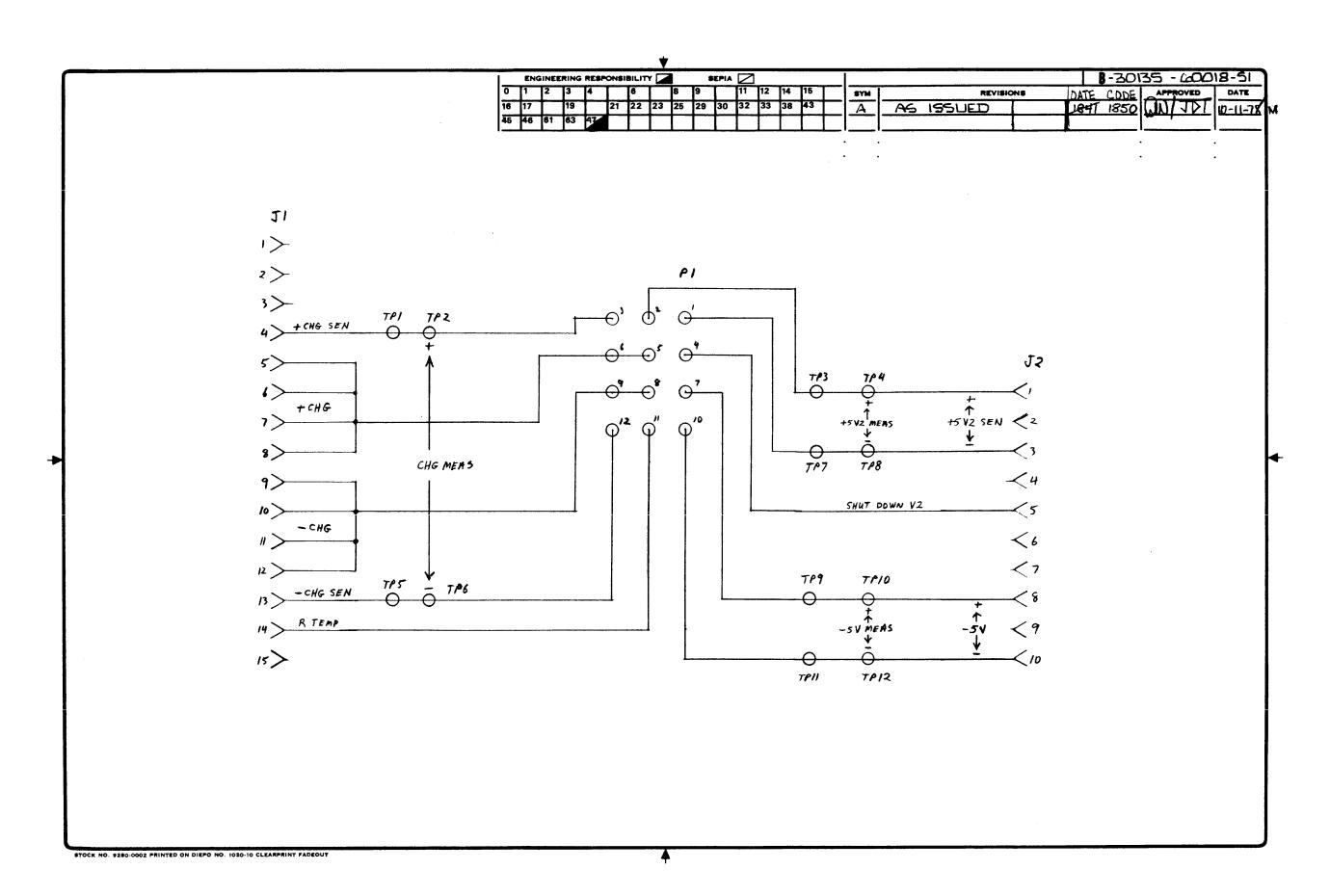
Table 1-6. HP 3000 Series III (32435A) PCA Slot Assignments

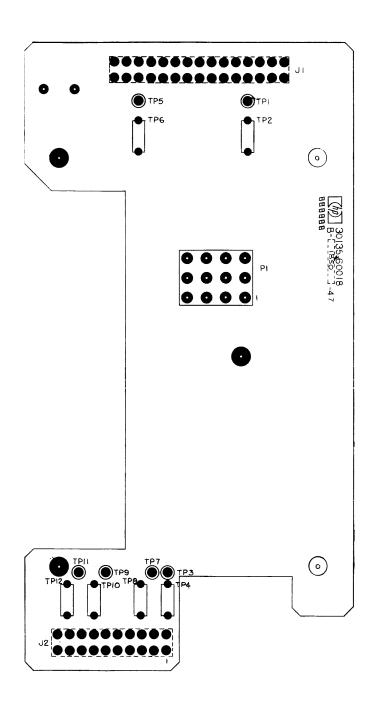
I/O BAY (OPTION 200)

	Slot	PRINTED CIRCUIT ASSEMBLY
CARD CAGE NO. 5	A1 A2 A3 A4 A5 A6 A7 A8 A9 A10	Available for programmed (SIO) or direct I/O
CARD CAGE NO. 5	A1 A2 A3 A4 A5 A6 A7 A8 A9 A10	Available for programmed (SIO) or direct I/O

CPU BAY

1	a .	
	Slot	PRINTED CIRCUIT ASSEMBLY
CARD CAGE NO. 1	A1	Reserved for maintenance panel PCA.
	A2	30012-60001 Extended Instruction Set
	A3	30003-60021 Read Only Memory
	A4	30003-60022 Skip and Special Field
	A5	30003-60003 Arithmetic and Logic Unit
	A6	30003-60004 R Bus
	A7	30003-60025 S Bus
	A8	30003-60006 Current Instruction Register
	A9	30003-60007 Module Control Unit
	A10	30003-60028 Input Output Processor
CARD CAGE NO. 2	A1	30008-60003 Memory Array (128K)
	A2	Available to add 128K
	A3	Available to add 128K
	A4	Available to add 128K
	A5	30007-60005 Memory Control and Logic #1
	A6	Available to add Memory Control and Logic #2
	A7	Available to add 128K
	A8	Available to add 128K
	A9	Available to add 128K
	A10	Available to add 128K
CARD CAGE NO. 3	A1	30135-60063 System Clock/FLI
	A2	30032-60001 Terminal Data Interface
	A3	30061-60001 Terminal Control Interface
	A4	30030-60020 Selector Channel Port Controller
	A5	30030-60021 Selector Channel Register
	A6	30030-60003 Selector Channel Control
	A7	30030-60011 Selector Channel Sequencer
	A8	Available for programmed (SIO) or direct I/O
	A9	Available for programmed (SIO) or direct I/O
	A10	Available for programmed (SIO) or direct I/O
CARD	A1	Available for programmed (SIO) or direct I/O
	A2	Available for programmed (SIO) or direct I/O
	A3	Available for programmed (SIO) or direct I/O
	A4	Available for programmed (SIO) or direct I/O
	A5	Available for programmed (SIO) or direct I/O
CAGE	A6	Available for programmed (SIO) or direct I/O
NO. 4	A7	30215-60002 Magnetic Tape Controller Processor
	A8	30215-60006 Magnetic Tape Controller
	A9	30036-60002 Multiplexer Channel
	A10	30229-60001 Disc Control Interface
L	L	





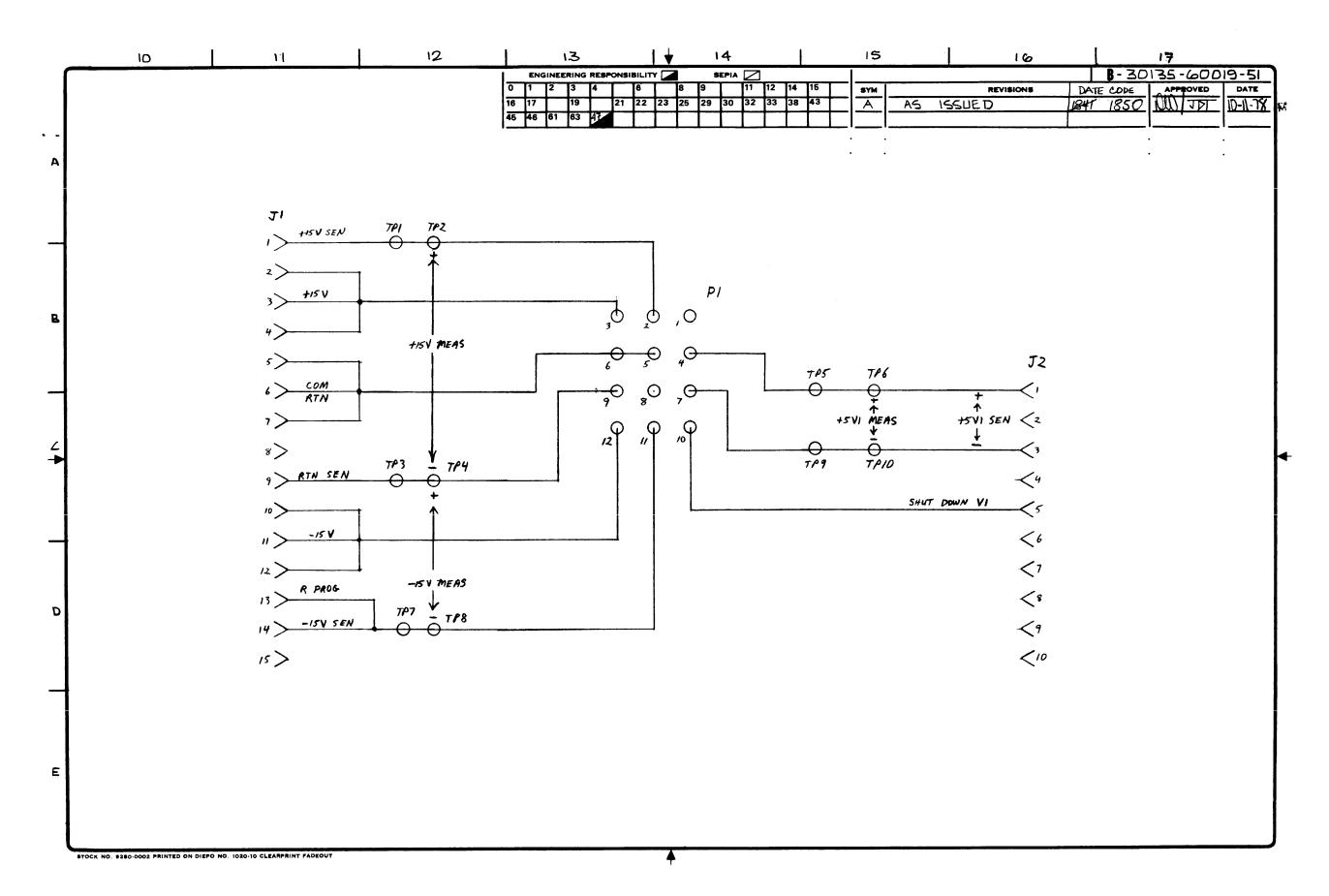
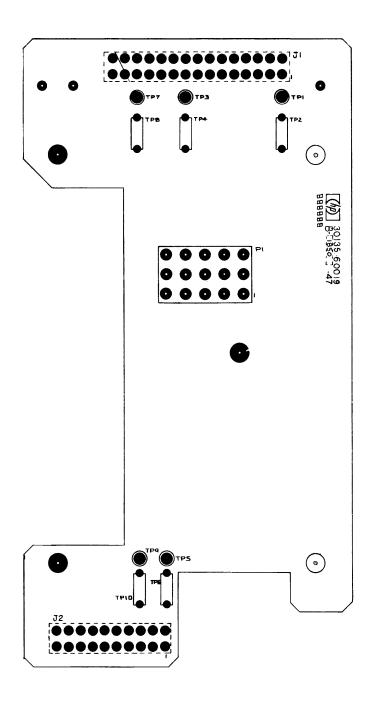


Figure 1-21. P02 Power Distribution PCA (32435A) Sheet 1 of 2



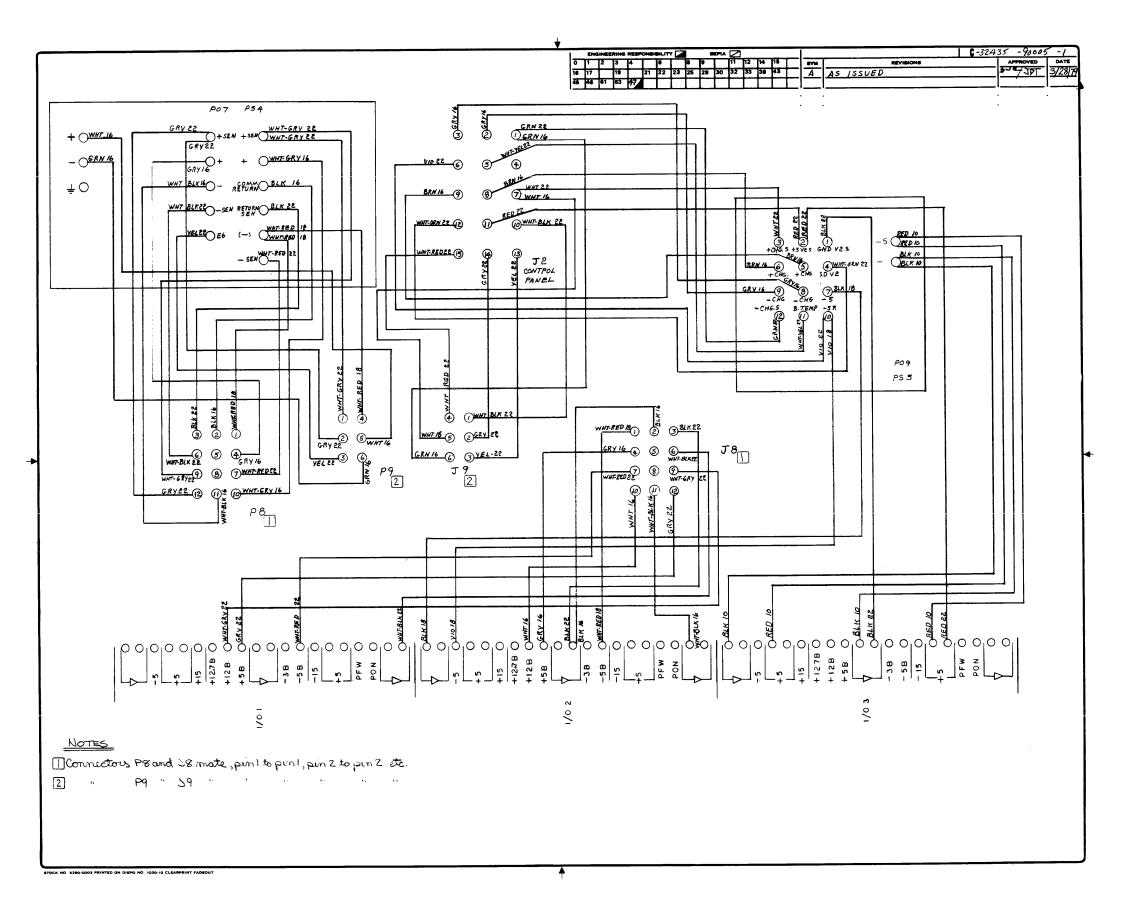
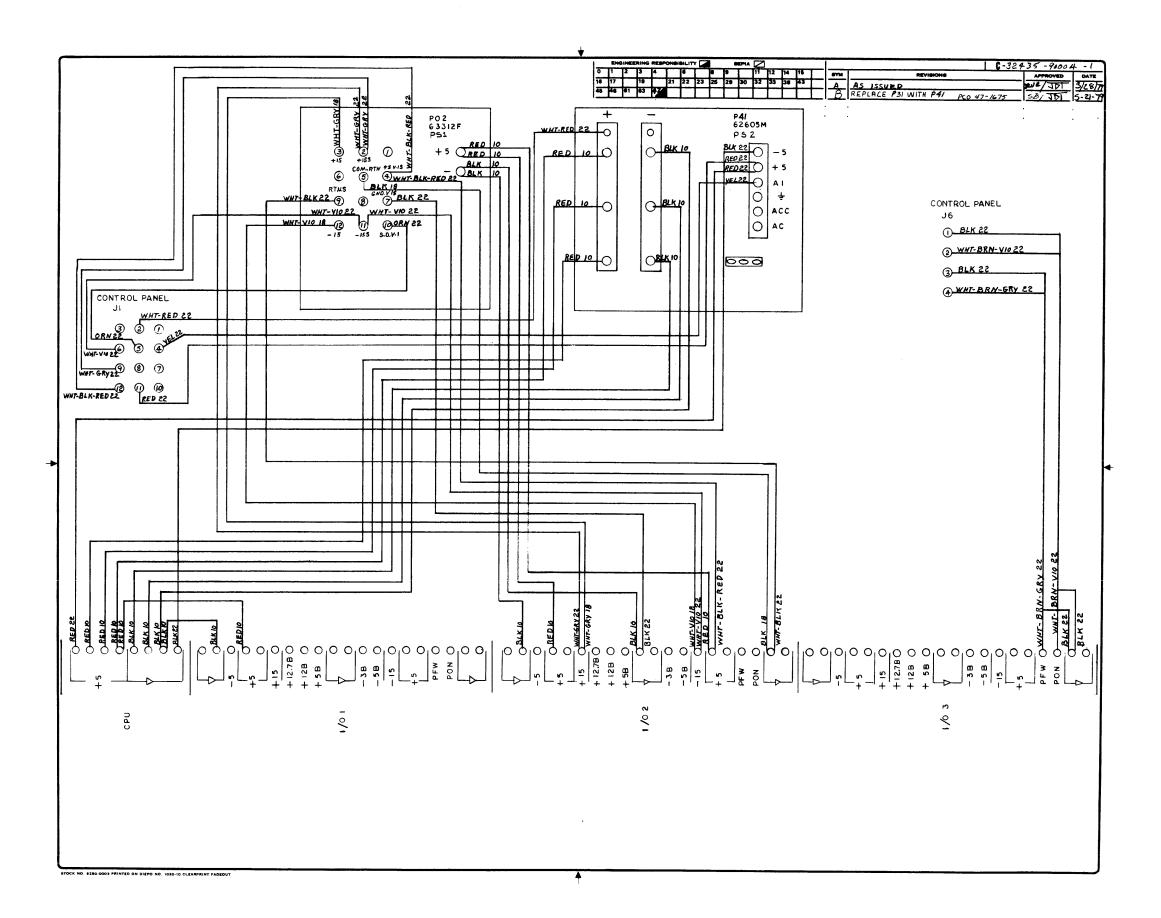
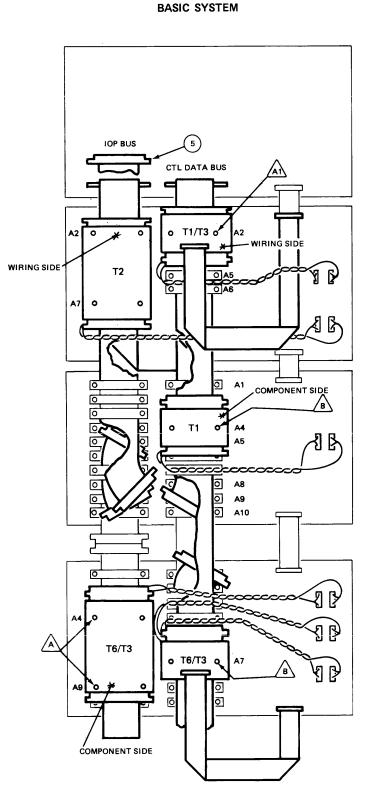
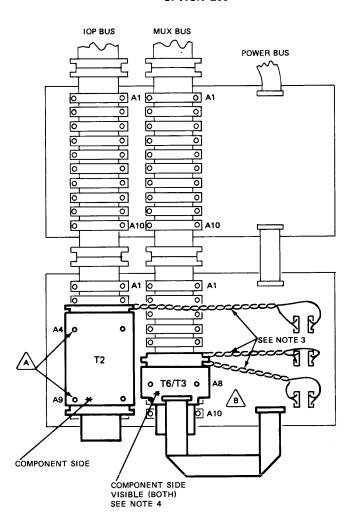


Figure 1-22. P07/P09 System Wiring Diagram (32435A)



OPTION 200





- 1. TERMINATORS ARE IDENTIFIED AS FOLLOWS: TERMINATOR QUANTITY PART NUMBE 30003-60030 30001-60016 30030-60015 30035-60003
- PRINTED CIRCUIT EDGE CONNECTOR J1 OF A TERMI-NATOR PLUGS INTO A FLAT CABLE CONNECTOR TO TERMINATE THE CABLE RUN. CORRECT TERMINATOR ORIENTATION IS ASSURED IF YOU KEEP PINS 49 AND 50 OF THE EDGE CONNECTOR TO THE LEFT WHEN TERMINATING THE FLAT CABLE.
- 3. EACH TERMINATOR HAS A RED TWISTED PAIR CABLE WHICH CONNECTS FROM EDGE P1 OF THE TERMINATOR PCA TO PINS 2 AND 1 (+5 VOLTS) ON ANY POWER BUS CONNECTOR P1. A BLACK TWISTED PAIR CABLE CONNECTS FROM THE PCA TO PINS 16 AND 15 OF THE SAME POWER BUS CONNECTOR.
- 4. T1/T4 = T1 IS BENEATH; T4 IS VISIBLE. T6/T3 = T6 IS BENEATH; T3 IS VISIBLE.

= DETAIL A, ITEMS 5,6,8

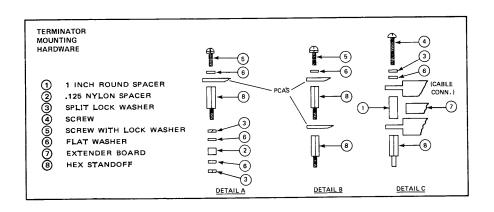
A1 = DETAIL A, ITEMS 2,3,5,6,8

B = DETAIL B

C = DETAIL C

= FLAT CABLE CONNECTORS JOINED WITH EXTENDER BOARDS

5. IF OPTION 200 PRESENT, IOP BUS EXTENDS TO CARD CAGE 5. OTHERWISE, TERMINATES AT 72.



047001-22

Figure 1-24. Flat Cable Terminators (32435A, with Option 200)

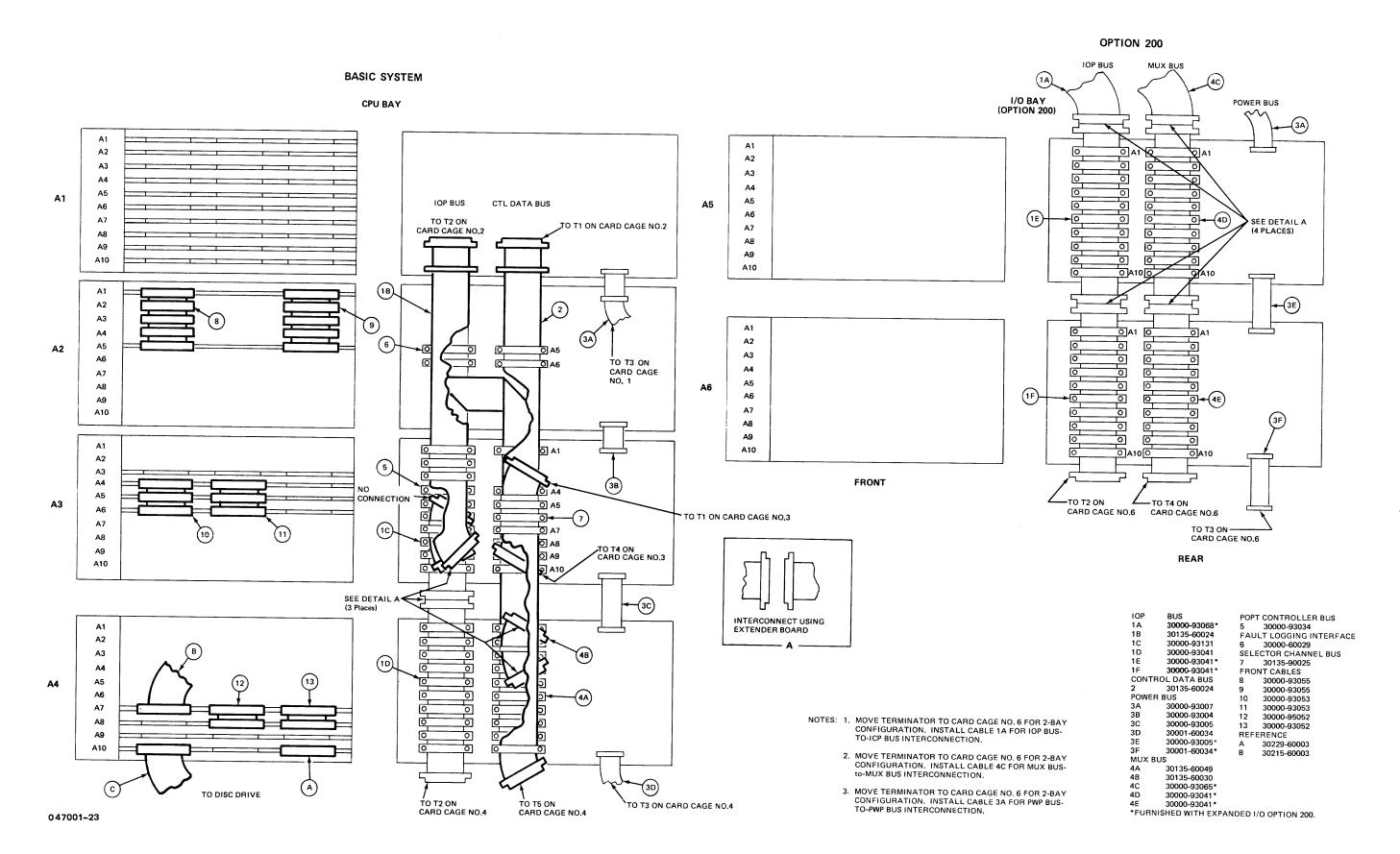


Figure 1-25. System Flat Cables (32435A, with Option 200)

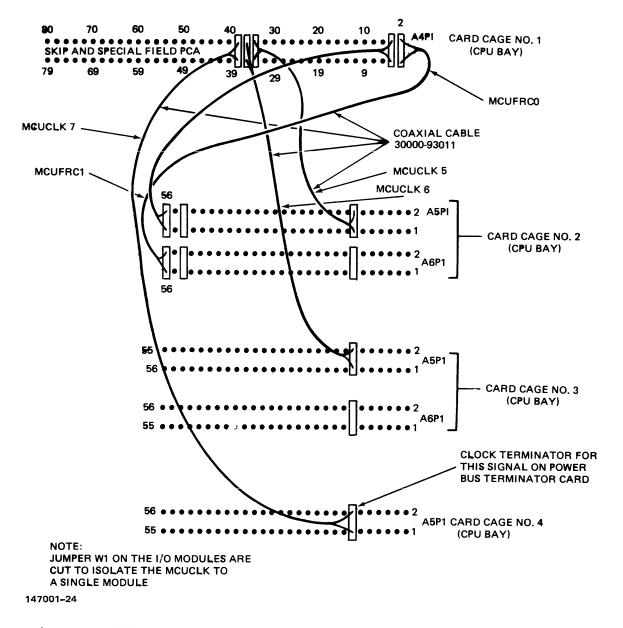


Figure 1-26. CPU Bay Clock Jumpers and Terminators (32435A)

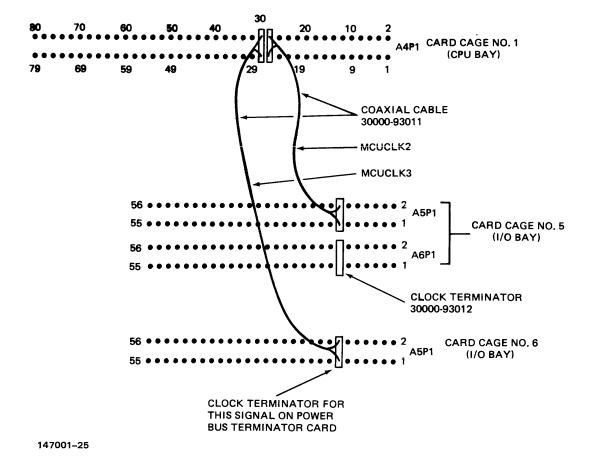


Figure 1-27. I/O Bay Clock Jumpers and Terminators (32435A)

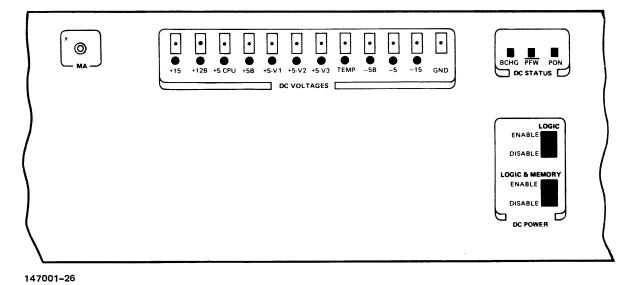


Figure 1-28. Power Control and Status Panel (32435A)

Table 1-7. Power Control and Indicator Functions (32435A)

Tubic i / Tower	00 (1= 1
Control or Indicator	Function
вснс	Lights steady for fully charged battery, blinks slowly while battery is charging, and blinks rapidly when battery is discharging. Remains unlighted when battery is fully discharged or is missing.
PFW	Lights when input AC power to the system is below specified value.
PON	Lights when AC power is applied to the power supplies and the power suplies are operating properly. Turns off when DC voltages decay because of power loss or a power supply fails.
LOGIC	When set to ENABLE, DC power is applied to all PCASs. When set to DISABLE, DC power is removed from all but memory PCAs.
LOGIC AND MEMORY	When set to ENABLE, DC power is applied to all PCAs, provided that the LOGIC switch is set to ENABLE. When set to DISABLE, all DC power is removed from

all PCAs.

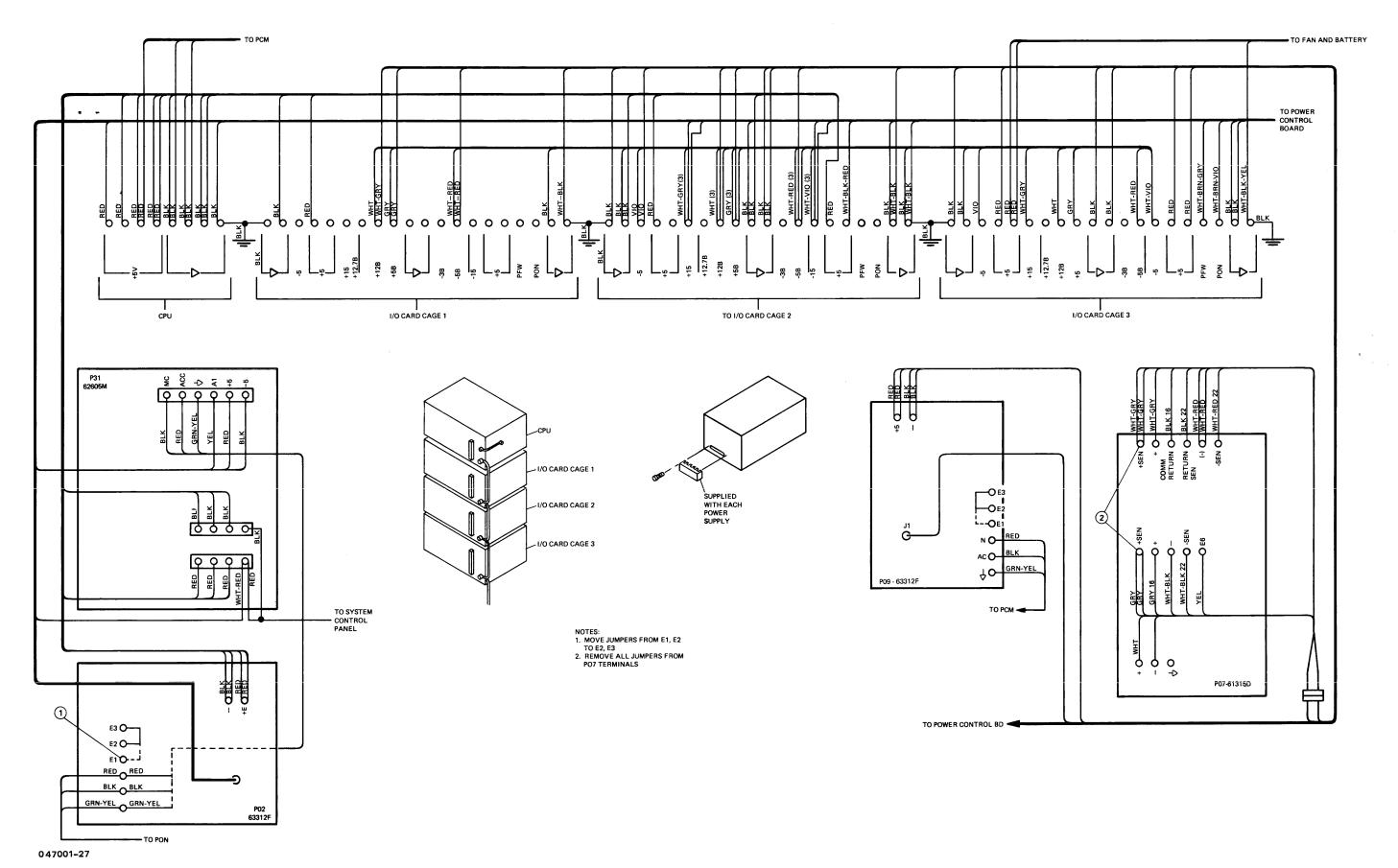


Figure 1-29. CPU Wiring (32435A)

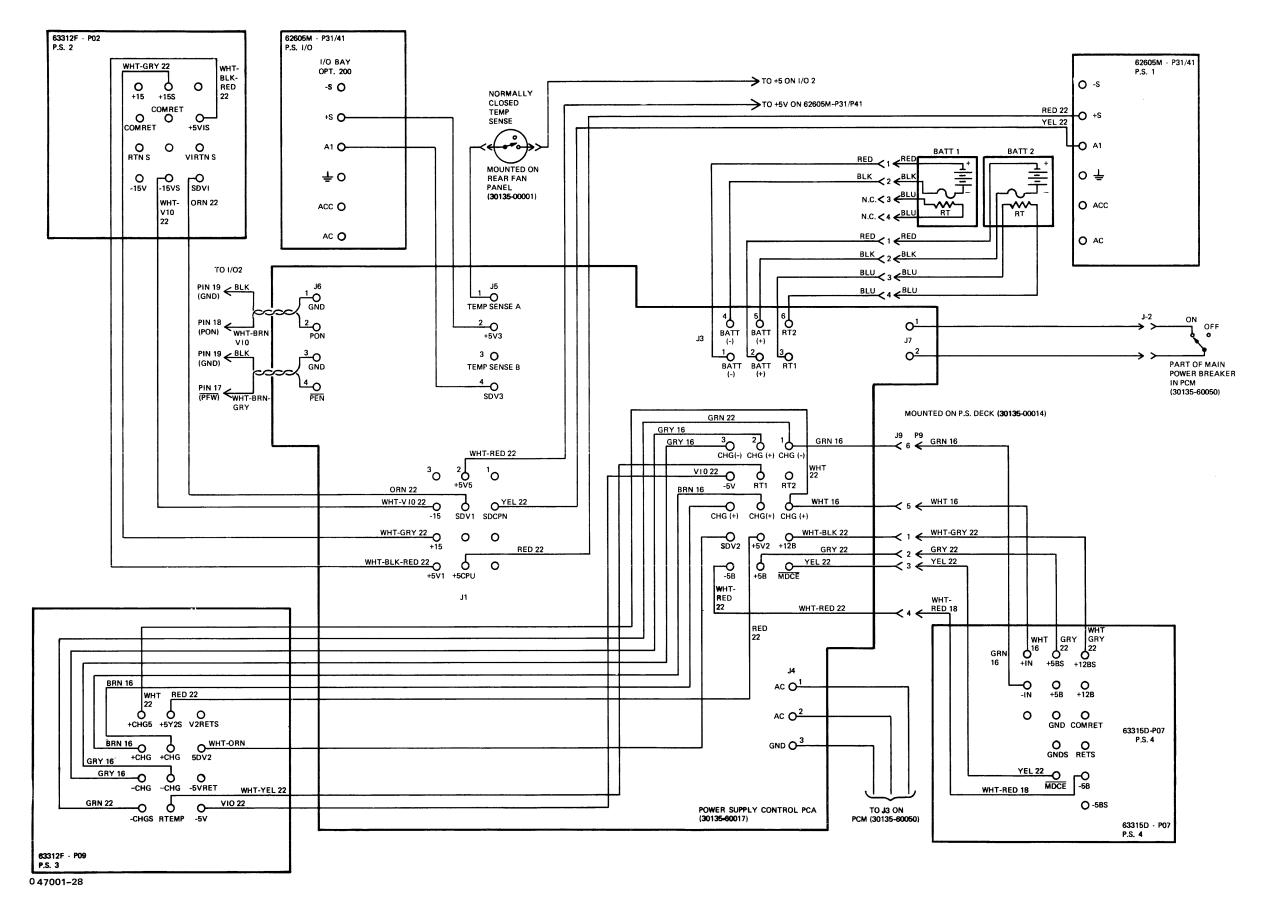


Figure 1-30. DC Power Connections (32435A)

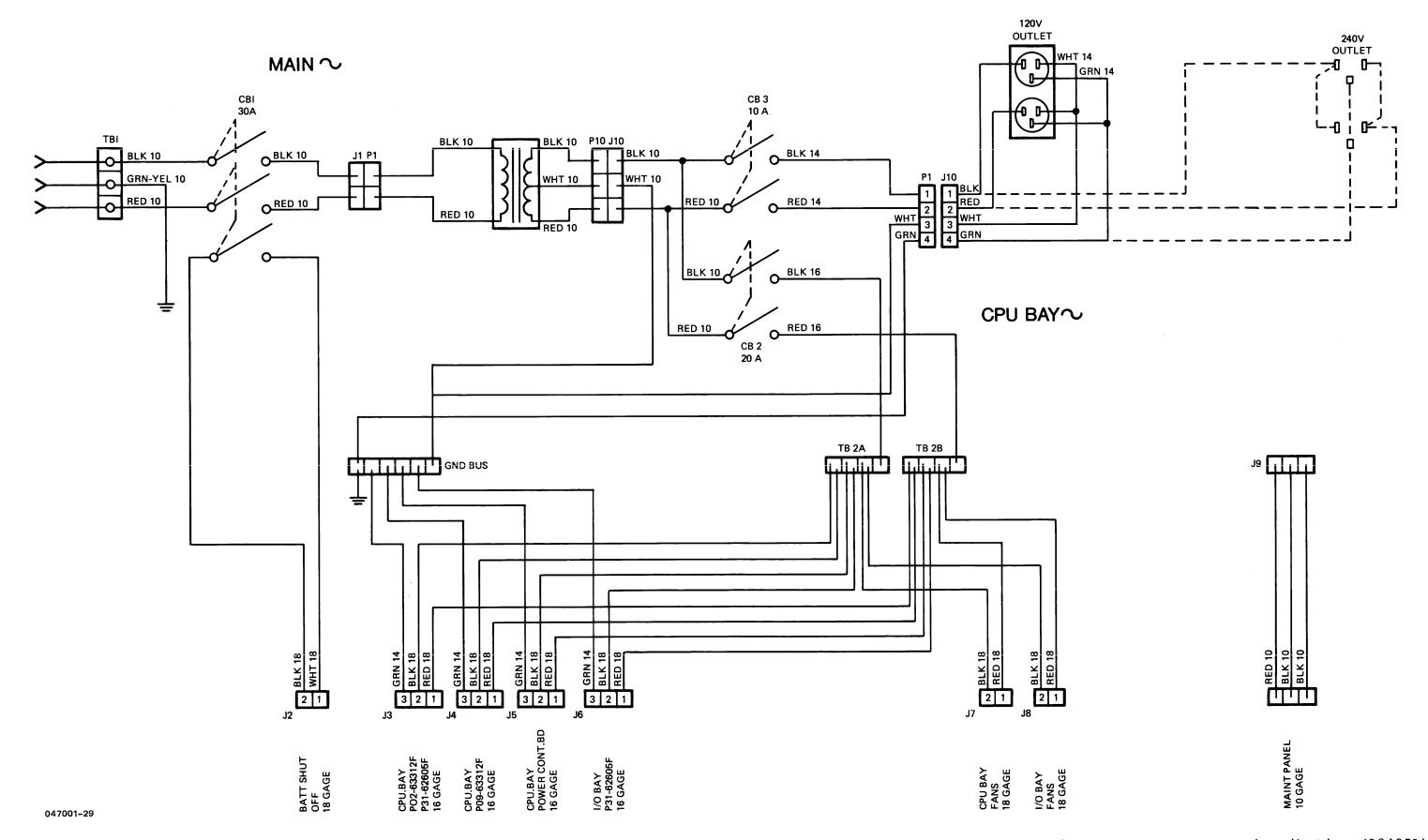


Figure 1-31. AC Power Distribution (32435A)

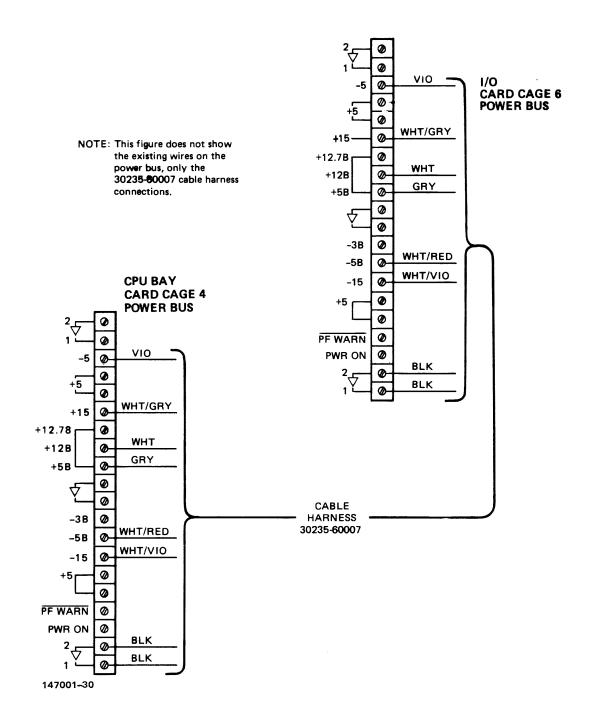
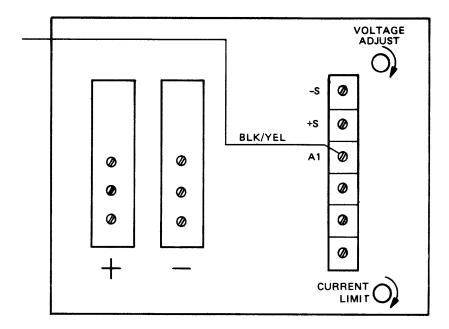
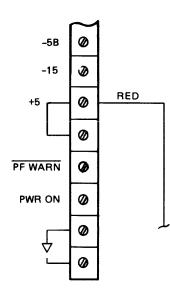


Figure 1-32. Cable Harness, 30235-60007, (32435A, with Option 200)





147001-31

Figure 1-33. Power Bus Connection (32435A, with Option 200)

Table 1-8. CPU Backplane Signal Distribution List

SIGNAL	1A 1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS	SIGNAL	1A 1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
-APE -BPINT -CARRY -CF3	P1*30 P1-65			P1-65 P2*18				P1-32	P2- 7	P2- 7	P2-47	-IOD11 -IOD12 -IOD13 -IOD14										P2*59 P2*61 P2*62 P2*63	P3-38 P3-39
-CLK	P1-78	P1-78				P1-78	P1-78	P1-78	P1-78	P1-78	P5- 2	-IOD15										P2*64	
-CLSR -CPUINH -CPULSEI -CPURST	P2-78	P2-78	P2-78	P1*15	P2*78 P2-71	P1-15 P2-78	P1-58 P2-78	P2-78 P2*69	P2-48 P1*61 P2-78	P2*48	P5 - 50	-IOD2 -IOD3 -IOD4 -IOD5 -IOD6										P2*41 P2*42	P3-24 P3-26
-DATAPE -DCTFRZ -DECSR -DEVN00			P1*22			P1-24		P1*11 P1-24	P1-11 P1-47	P1*47	P3- 8	-IOD7 -IOD8 -IOD9										P2*45	P3-30 P3-32 P3-33
-DEVNOO											P3- 9	-IODPRTY										P2* 9	P3- 1
-DEVN 02 -DEVN 03 -DEVN 04											P3-11 P3-12 P3-14	-IOPACT -IORESET -IORSTSW					P2*79 P2-70			P2*68	P1-22 P2-79	P2-79	
-DEVN05 -DEVN06										P2*28 P2*29	P3-15 P3-17	-IOSTEP -IOSTROP	P1*45								P1*17	P1-44 P1-12	
-DEVNO7 -DISPLAY -ENB -ERFRZEI -EXTRP		:	P1-68	P1-68		P1-68			P1-68 P2*18 P1-12	P2*30 P1-15	P3-18	-IOTIMER -IOX12 -IOX13 -IOX14 -IOX15									P1*29	P2-10 P2-67	P3-45 P3- 2 P3-47 P3-48
-FCLK -FHB -FIELD6 -FIELD8 -FIELD9	P1-79	P1-79	P1-79		P1-79 P1-59 P1*34 P1*35 P1*32	P1-79	P1-79	P1-79 P1-15 P1-31	P1-79	P1-35	P5- 4	-JBNDV -JLUT1 -JMPFRZ -JMPJSB1 -JSB1	P1 - 54		P1*18 P2*23 P1*15	P1-12 P1*56 P2-28	P2*66	P2-28			P1-31		
-FRCLK -FRUNCL -FRZ -HSREQ -INCSR	K P2-35 P1-51			P1*10 P2*32 P1-50		P1-27		P1-27	P1*46	P1-46 P1-37	P1-12	-LDACOR -LDDCOR -LSRSPO -MCUCLOR -MCUCLIR	P2*23		P2-30	P1*24 P1*26			P1-66 P1-50		P1*66 P1*50		
-INCT -INTACK -INTREQ -INTRP1 -IOCMD0				P2*74 P2-52			P2-77	P2*58		P2*65	P3-50 P3-44 P3-4	-MCUCL2R -MCUCL3R -MCUCL4R -MCUCL5R -MCUCL6R				P1*28 P1*30 P1*32 P1*34 P1*36							
-IOCMD1 -IOCMD2 -IOD0 -IOD1 -IOD10										P2*31 P2*32	P3- 6 P3- 5 P3-20 P3-21 P3-35	-MCUCL 7R -MCUCLK0 -MCUCLK1 -MCUCLK2 -MCUCLK3				P1*38 P1*23 P1*25 P1*27 P1*29							

Table 1-8. CPU Backplane Signal Distribution List (Continued)

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS	SIGNAL	1A 1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
-MCUCLK4				P1*31 P1*33								~SYSPE -T=0				P1-74	P1*74				P2*27	P2- 8	P2-48
-MCUCLK6 -MCUCLK7				P1*35 P1*37								-TESTFR: -TINT	Z	P2*56							P1-32		DE /0
-MCUFR1R				P1* 4								-TMRUFR	Z	1250			P2*59				P2-56 P1-45		P5-48
-MCUFRCO				P1* 1								-TRO						P1*34	P1-34				
-MCUFRC1				P1* 3								-TR1						P1*35	P1-35				
-MCURST -MODINH									P2* 1		P2-49	-TR2						P1*36					
-MODINHR									P2-41 P2-42			-TR 3 -UNC 1			P1* 5	P1- 5		P1*3/	P1-37				
									12-42			01101			11. 3	11- 3							
-MPIFRZ	P1*34								P1-33			- V0		P2-11						P2* 7			P5-10
-NEXT1	DO 20		P1* 6	P1- 6				-0.50				-V1		P2-12						P2* 8			P5-12
-NOP -NOP2	P2-38			P2-70 P2*77	D2 77	D2 77		P2*70	D0 76			-V10		P2-31						P2*31			P5-30
-NOF 2 -NXTG			P1-66	FZ*//	P2-77	P2-77 P1*67			P2-76			-V11 -V12		P2-32 P2-33						P2*32			P5-32
112120			11 00			11.07						-V12	F2*33	r2 - 33	FZ*33					P2*33			P5-34
-OVFL	P1-53				P1-53	P1*44						- V13	P2*34	P2-34	P2*34					P2*34			P5-36
-PADDX						P2-79		P2*79				- V14		P2-41						P2*41			P5-38
-PANLRD	P1-56		P1*56	P1-54	71.0 4							- V15		P2-42						P2*42			P5-40
-PFWARN -PNLS	P2-12		D21 /	P2-14	P1-24						P1- 2	-V2		P2-13						P2* 9			P5-14
-1 MLS	12-12		F2-14	r2 - 14	FZ*11							-V3	P2*16	P2-16	P2*16					P2*12			P5-16
-POLORSO									P1-26	P1*26		- V4	P2*18	P2-18	P2*18					P2*18			P5-18
-RBR1			P1*55	P1=52			P1-28				-	- V5		P2-17						P2*17			P5-20
-RDIOA					D0+60		P1*64			P1-64		- V6		P2-27						P2*27			P5-22
-REPN -REVMCUP					P2*68 P1*43		P2-65 P1-56					-V7		P2-28						P2*28			P5-24
KLVHOOT					11.45		11-50					-V8	PZ*29	P2-27	P2-29					P2*29			P5-26
-ROMFCN1			P2*22			P2-24						- V9	P2*30	P2-30	P2*30					P2*30			P5 - 28
-RORT15				P2-36								A0					P2*29		P2-29				
-RORT16 -RORT21				P2-38	DO 20							A1					P2*30		P2-30				
-ROR121			P2*37	P2- 3	P2-32				•			A15 ALPHA				D2 12	P2*34	D0410	P2-34				
KOD I			12. 3	12 3								ALITA				P2-12		P2*12					
-SAME				P1-75	P1*77							AT01							P1* 1		P1- 1		
-SBR				P2-48		P2*46						ATO2							P1*10		P1-10		
-SETERR					P1*36				P1-36	P1-36		B12				P1*24			P1-30				
-SF3				P2*17	P2-17	D0 //	D04//					B13	DO 7			P1*23			P1-12				
-SFQ0						P2-44	P2*44					B14	P2- 7			P2* 7			P2- 7				
-SI									P1*41	P1-41	P1-16	B15	P2- 8			P2* 8			P2- 8				
-SIFRZ										P1*34		BCMP							P2*63	P2-62			
-SIFRZ										P1*34		BMCUPRT	7								P1-75	P1*66	
-SIOCMP -SLOAD	P1*13				P1_13	P1-13		D1_13	P1-27 P1-13	P1*28		BMUX	DO 1/				D0407			P1* 1			
DLOID	11 13				1113	11-13		11-13	11-13	11-13		BNDV	P2-14				P2*27			P2-71			
- S0										P1*43	P1-18	BPENDING	}			P2-54				P2*52			
-SPBBANK				P1-57			P1-62		P1*65	D1 00		BUSOP1			P1*70						P1-72		
-STEPENR -STTR	L1*30					D1 # 2 0	P1-38			P1-32		CB14							P2*12				P2-31
-STIR -SWLDRAR	P2*13			P2-26		L1,20	L1-20	P2-11				CB15 CCPX	P1-16			D1 41 6	P1-16		P2*32	D1 17		P2-73	P2-45
	10											OULV	11-10			LT.10	L1-10			P1-16			

Table 1-8. CPU Backplane Signal Distribution List (Continued)

										*		<u> </u>												
SIGNAL 1A	A 1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS		SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
CIR12			8			P1-58		P1*58					INTCLKM	P1*64			P1-64				P2-51			
CIR13						P1-57		P1*62					INTG INTPOLL	P2-22			P2*50				12-31		P1*79	
CIR14						P1-65 P1-66		P1*64 P1*66					INTRP	P1-63			P2-51				P2*66			
CIR15 CIR4						P1-66 P1-49		P1*49					IOERR									P2-50	P2*50	
								71.150					IOHR									P2-58	P2*58	
CIR7					P1-48			P1*50 P1*56					IOHREQ										P2-57	
CIR8	1-67				P1-56	P1-76		1130	P1-42	P1-48	P1-48	3	IOHSEL										P2-53	
	1*61				P1-61	11 ,0							IOINP	P2-49								P2*56 P2-70		
	2-51								P2*64				IOLR									12-70	12.70	
GAZETA A W				P2-59			P2*59						IOLREG									P2*68		
CNTRMAX CPUIN				12-33			12 37	P1-38	P1*38				IOLSEL									P2*54 P2-51	P2-54 P2*51	
CPUSEL							P1-24		P1*24				IOMOP0									P2-51 P2-52		
CUPTIMER P1-	-29				P1*33			P1-29	P1-30				IOMOP1									12-32	P1*33	P1- 8
DATAPOLL										P1* 1			IORESET											
DISPFLG P1-	-46				P1*46			P1-46					IOSEL									P2*59	70 FF	
DPOP	-40					P1-72			P1*71				IOSPE									P2*55 P2-74		
DS						P2-27		P2*25					IOTO1									P2-74 P2-72		
DVSB				P2-56	P2*57								IOTO2				P2*71				P2-54	12 /2	1	
EMULATOR			P1*30				P1-25		P1-16 P1-70	D1 *62			JLUIM				12 /1							
ENABLE									11-70	11.02			JMP1G	P1-72			P1*72					-0 //		
ENABLEO								P2-15		P2-40			JMP2G	P1-62		P2-43	P2*45					P2-44		
ENABLE 1								P2-19		P2-41			LDBREG	P1*70			P1-66 P2*72				P2-73			
ENABLE 2								P2-17		P2-42	2		LUTG MCUCMP	P2-79 P1-42			FZ~72				P1*41			
ENABLE 3								P2-23 P2*21		P2-43 P2-44			MCOCM	11-42										
ENABLE4								PZ*21		r 2-44			MCUD0								P1-55			P2- 2
ENTIMER P1	L * 31				P1-31				P1-44		P1- 1	l	MCUD1								P1-59		P1*59 P1*76	
EXTCLK				P1-67									MCUD10								P1-76 P1-70		P1*70	
EXTINT								P1-10		P1*10			MCUD11								P1-68		P1*68	P2-16
	2- 1			P2* 1	P2- 1 P1*27	P2- 1		P2- 1	P1-14				MCUD12											
FIELD2					P1*27				11-14				MCUD13								P1-73			P2-17 P2-18
FIELD4					P1*29				P1-21				MCUD14								P1-71 P1-77			P2-19
FIELD5					P1*28				P1-19				MCUD15								P1-57			P2- 4
FIELD7					P1*26				P1- 8				MCUD2 MCUD3								P1-63			P2- 5
	1-58				P1-58 P1-73								HOODS								(1		D1461	D2 6
FLAG2 P1	1–73			1175	11 73								MCUD4								P1-61 P1-65			P2- 6 P2- 7
FLAG3 P2	2-37			P2-37	P2*33							_	MCUD5								P1-69			P2- 9
FROM0									P2*16 P2*22		P2-2 P2-2		MCUD 6 MCUD 7							P1*67	P1-67			P2-10
FROM 1									P2*22 P2*12		P2-2 P2-2		MCUD8							P1*74	P1 - 74		P1*74	P2-11
FROM 2 GND											_									D1 + 70	P1-72		P1*72	P2-12
0.1.D													MCUD 9							P1*72 P1*75	r 1-/4			P2-20
	1-47				P1*47			P1-47					MCUDPR7	ĽY						1113	P1-25	P1*25		
ILGADR				D1410		D1 14	P1*29		P1-28				MCUERR MCUFRZ					P1-37				P1*18		
INCNAMER				P1*13 P2*19		P1-16	P2-25						MEMREF						P1-48		P1*48			
INCP INDIRECT				P2-73				P2*72																
THETHOT																								

Table 1-8. CPU Backplane Signal Distribution List (Continued)

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS	SI	GNAL	lA1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
MODINT MOPO MOP1 MPICO MPIC1	P2* 5 P2* 6			P2-47 P2- 6				P1- 9	P1* 7 P2*14 P2*10		P2-28 P2-29	R3 R4 R5 R6 R7				P1*10 P1*61 P1*62 P1*63 P1*64		P1-61 P1-62 P1-63	P1*10 P1*61 P1*62 P1*63 P1*64					
NAMERO NAMER1 NEXT NIP NIPO	P1-43			P2*43	P2-41	P1*25 P1*26	P2-42	P2-44 P1-43	P1*43 P1* 9			R 8 R 9 R A I R A I R D O	RGA RGB	P2-47 P2-15		P2*10 P2* 9 P2-46 P2-15		P2-10 P2- 9	P2*10 P2* 9 P1*28		P1 - 28			
NIPSEL NIRTOCIR NOP2 NOTUSED NUMERIC	P2-76			P1*49 P2*76 P2-16	P2-76	P2*17	P2-76	P1-37	P1*64 P1-37		P1-10	RDO RDI RDI	CPX1 CPX2 IOD IOD OPND							P2*45 P2*47 P2*46	P2-43 P2-45 P2-49	P2-46	P2-47	
NXT+1 OFCENB OPINP OPNDSEL OVFLINT	P2-59 P1-35			P2*67 P2-69 P1*63	P2*69	P2-64		P2-67 P1-35 P1-26	P1*35 P1*63			REA REA REA	SWITCH ADYO ADY1 ADY2 ADY3							P2*50	P2-50	P2*31 P2*32 P2* 9 P2*29		P2-33 P2-34 P2-35
PADDIN10 PADDIN11 PADDIN8 PADDIN9 PADDSUB						P2-57 P2-59 P2-53 P2-55 P2-61		P2*57 P2*59 P2*53 P2*55 P2*61				REA REA REA	ADY4 ADY5 ADY6 PEAT /SYSP	P2-21			P2*21	P1*38				P2*13 P2*11 P2*30		P2-36 P2-37 P2-38 P2-31
PADDXS 00 PADDXS 01 PAUS E PONB PONUB				P2 - 41	P2*74 P2*45	P2-63 P2-65 P2-76		P2*63 P2*65 P1*45 P2-74				RFO RF1 RF2 RF3) 	P2*56 P2*54 P2*52 P2*50		P2*56 P2*54 P2*52 P2*50		P2-58	P2*56 P2*54 P2*52 P2*50			P1-73		
PWRFAIL PWRON QASL QASR QDWN					P1*30 P1-25 P2*64 P2*62	P2-62 P1*31	P2-64 P1-31	P1-30			P1- 6	RMO RMO ROM ROM ROM)P0)P1 (0	,	P1* 3	P1* 4 P1* 3 P1*32		12 30	12.50			P2*33 P2*34		P4- 2 p4- 3 P4-17
QS R0 R1 R10 R11		•	P1*12 P1*11 P2* 8 P2* 7	P2-29	P1-12 P1-11 P2- 8 P2- 7	P1*11 P2* 8		P2*26				ROM ROM ROM ROM	112 113 114	: : :	P1*33 P1*35 P1*34 P1*36	P1*33 P1*35 P1*34 P1*36 P1*38								P4-18 P4-20 P4-21 P4-23 P4-24
R12 R13 R14 R15 R2]]]	P2*47 P2*48 P2*49 P2*51 P1* 9		P2-47 P2-48 P2-49 P2-51 P1- 9	P2*48 P2*49 P2*51						ROM ROM ROM ROM	17 18 19]]]	P1*42 P1*43 P1*44	P1*41 P1*42 P1*43 P1*44 P1*21								P4-27 P4-28 P4-30 P4-31 P4- 5

Table 1-8. CPU Backplane Signal Distribution List (Continued)

SIGNAL	1A 1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS	SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
D07430		D1 4/5	P1*45								P4-33	RORT27	P2-77		P2*77	P2-75					P2-77		
ROM20			P1*46								P4-34	RPTFCN				P2-10	P2*12						
ROM21 ROM22		P1*47									P4-36	RREGO				P1-51							
ROM23			P1*48								P4-37	RUNFF	P1-36						P1-26	P1*34			
ROM24		P1*51									P4-39	S0					P1- 3	P1* 3	P1* 3	P1* 3	P1* 3	P1* 3	
ROM25		P1 * 52	P1*52								P4-40	S1					P1- 4	P1* 4	P1* 4	P1* 4	P1* 4	P1* 4	
ROM26			P1*53								P4-42	S10					P2- 5	P2* 5	P2* 5	P2* 5	P2* 5	P2* 5	
ROM27			P1*54								P4-43	S11					P2- 6	P2* 6	P2* 6	P2* 6	P2* 6	P2* 6	
ROM28			P1*65								P4-45	S12					P2-38	P2*38	P2*38	P2*38	P2*38	P2*38	
ROM29			P1*67								P4-46	S13					P2-37	P2*37	P2*37	P2*37	P2*37	P2*37	
ROM3		P1*24	P1*24								P4- 6	S14						P2*36	P2*36	P2*36	P2*36		
ROM30			P1*69								P4-48	S15						P2*35	P2*35	P2*35	P2*35		
ROM31			P1*71								P4-49	S2						P1* 5	P1* 5	P1* 5	P1* 5		
ROM4		P1*23	P1*23								P4- 8	S3							P1* 6	P1* 6	P1* 6		
ROM5			P1*25					*			P4- 9	S 4					P1-54	P1*54	P1*54	P1*54	P1*54	P1*54	
ROM6		P1*27	P1*27								P4-11	S5						P1*53	P1*53		P1*53		
ROM7			P1*26								P4-12	S 6					P1-52	P1*52	P1*52	P1*52	P1*52	P1*52	
ROM8			P1*28								P4-14	S 7					P1-51	P1 * 51	P1*51	P1*51	P1*51	P1*51	
ROM9			P1*31								P4-15	s8						P2* 3	P2* 3	P2* 3	P2* 3	P2* 3	
ROMENB			P2- 6								P5- 8	S 9					P2- 4	P2* 4	P2* 4	P2* 4	P2* 4	P2* 4	
ROMFNCT2)				P1*67				P1-67			SAVEG	P2-45		P2-44	P2*44							
ROR10	-		P1*72		P1-66							SCMD	P1-52									P1*50	
ROR 11			P1*73		P1-68							SDFG				P1*71	P1-70						
ROR12			P1*74		P1-71							SF0	P2*66		P2 * 66				P2-66				
ROR13			P1*75		P1-72							SF1	P2*68		P2*68			P2*68	P2-68				
ROR14			P1*76		P1-75							SF2	P2*70		P2*70				P2-70				
ROR23			P2* 5	P2- 5								SF3	P2*72		P2*72				P2-72				
ROR23				P2-24								SF4	P2*74		P2*74			P2*74	P2-74				
RORT10	P2-44	i	12 27		P2*44							SFSAME					P2-28		P2*28				
	P2-43				P2*43							SHIFTCLE	C P1*23				P1-23	P1-23		P1-23	P1-23	P1-24	
RORT12	P2-2	1			P2*24							SIFG				P1*69	P1-69						
RORT13	P2-25				P2*25							SIODR	P1-48									P1*49	
RORT14	P2-46				P2*46							SIODR	P1-24									P1*30	
RORT15	P2-53		P2*53	P2-53			P2-53					SIOMAP	PR-25									P1*31	
RORT16	P2-5			P2-55			P2-55					SIOP	P1- 9									P1* 9	
RORT17	P2-58	3	P2*58	P2-58			P2-58					SKIP	P2-26			P2*27		P2-26					
RORT18	P2-5			P2-57			P2-57					SKIPNOP			P1*13	P1- 9				D1 400			
RORT19	P2-62			P2-62			P2-62					SMCO	P1-27							P1*33			
RORT20	P1-5		P1*57		P1-57							SP1 0						P1* 1					
RORT21	P1-49		P1*49		P1-49							SP115					P2-31	P2*30					
RORT22	P1-50)	P1*50		P1-50							SPlin						P2-42					
RORT23	P2-6			P2-61					P2-61			SP1SHIF	Г					P1-45					
RORT24	P2-6			P2-63					P2-63			SP3 0					P2-54		P2*54				
RORT25	P2-6			P2-64					P2-64			SP315						P2-25					
RORT26	P2-6		P2*65	P2-65					P2-65			SP3IN					P1*15		P1-15				

Table 1-8. CPU Backplane Signal Distribution List (Continued)

SIGNAL	1A 1	1A2	1A3	1A4	1A5	1A6	1A7	1 A 8	1A9	1A10	BUS
SP3SHIFT SPCLNOP1 SPETFM	P1-66		P2*25	P2-25	P2*61		P2-61		P2*66		
SRO SR1				P2-34 P2-33		P2*34 P2*33		P2-47 P2-48			
SR2 SRBUS SRDYENB SRREG	P1-44 P1-69 P1-71			P2-31	P2*52	P2*31 P1*44		P2-46	P1*69		
SSBUS	P1-41					P1*41					
SSREG STO ST1 ST2 ST3	P1-76 P2*67 P2*69 P2*71 P2*73		P2*67 P2*69 P2*71 P2*73		P2*50	P2-67 P2-69 P2-71 P2-73					
ST4 STATUS 0 STATUS 1 STATUS 2 STATUS 3	P2*75		P2*75	P1*41 P1*42 P1*43 P1*44	P1-41	P2-75	P2-75 P1-41 P1-42 P1-43 P1-44	P1-44	P1-42	P1-42	
STATUS 4 STATUS 5 STATUS 6 STATUS 7 STBUS OP				P1*45 P1*46 P1*47 P1*48 P1-62			P1-45 P1-46 P1-47 P1-48		P1*62		
STIOA STIOD STORAR STSTATUS SUBF	P2-48			P1-70 P2-79 P2*49		P1*70	P1*11 P1*16 P2*79	P2-77		P1-11 P1-16	
SUBUS SYSPIN SYSPRTY TO	P1-55			P1-55	P1 * 55	P1*55	P1-49 P2* 9		P1-49 P2- 8		P2-32
	P1-32				11 33	P1*32	P1-32				
TNAMP01 T00 T01 T02	P1-33					P1*33	P1-33		P2*28 P2*24 P2*26		P2-22 P2-23 P2-24
Π0	P1- 8			P1- 8	P1* 8	P1- 8	P1- 8	P1- 8		P1- 8	-
U1 U10 U11 U12 U13	P1-14			P1-14	P2*15 P2*16		P1-14 P2-15 P2-16 P2-19 P2-21		P1-55 P1-56 P1-57	P1-14 P2-15 P2-16 P2-19 P2-21	

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
U14 U15 U2 U3 U4	P2-19			P2-22 P2-23 P1- 7 P1-17 P1-18	P2*22 P2*23 P1* 7 P1*17 P1*18	P2-22 P2-23 P1- 7 P1-17 P1-18	P2-22 P2-23 P1- 7 P1-17 P1-18	P2-22 P2-23 P1- 7 P1-17 P1-18	P1-58 P1-59	P2-22 P2-23 P1- 7 P1-17 P1-18	
U5 U6 U7 U8 U9				P1-19 P1-21 P1-22 P2-13	P1*19 P1*21 P1*22 P2*13 P2*14	P1-19 P1-21 P1-22 P2-13 P2-14	P1-19 P1-21 P1-22 P2-13 P2-14	P1-19 P1-21 P1-22 P2-13 P2-14		P1-19 P1-21 P1-22 P2-13 P2-14	
UGATF VBUSENB W XSW12 XSW13	P2-36 P1-74	P2- 4	P2- 4	P2*35 P2- 4			P1-13 P1-23	P2-24 P2-10 P2*76			P5- 6
XSW14 XSW15	P1*75 P1*77			P2-11 P1-77			P2-11 P2-10				

Table 1-9. IOP Power Bus (non-Memory Card Cage)

PIN	NUMBER	SIGNAL	PIN N	IUMBER	SIGNAL
56-PIN	20-PIN		56-PIN	20-PIN	
1		+5V	30		
1 2 3		+5V	31		Not used
		+5 V	32		Not used
4		+5V	33		Not used
5		PF WARN	34		Not used
6	1	ENTIMER	35		Not used
7	4	Spare	36		Not used
8	3	Spare	37		Not used
9	6	PWR ON	38		Not used
10	5	PWR ON	39		Not used
11	8	IORESET	40		Not used
12	7	IORESET	41	12	HSREQ
13	10	MCUCLKS 2	42	11	
14	9	MCUCKKS	43		1
15			44		1
16			45		IODPE
17		-5 V	46		
18		- 5V	47		1
19			48		1
20			49	16	SI
21			50	15	SI
22			51		1
23		Not used	52		1
24		Not used	53	18	80
25		Not used	54	17	S 0
26		Not used		55	1
27		Not used	56		1
28		Not used		20	Not used
29				19	Not used

¹ Reserved for interrupt and data poll connections at backplane.

Table 1-10. Central Data Bus

 PIN	 SIGNAL 	 PIN 	SIGNAL
1	COM	26	FROM1
1 2 3	MCUDO	27	FROM2
3	MCUD1	28	MOPO
4 5	MCUD2	29	MOP1
5	MCUD3	30	COM
6	MCUD4	31	CB14
7	MCUD5	32	SYSPRTY
8	COM	33	READYO
9	MCUD6	34	READY1
10	MCUD11	35	READY2
11	MCUD8	36	READY3
12	MCUD9	37	READY4
13	MCUD10	38	READY5
14	COM	39	COM
15	MCUD11	40	ENABLEO
16	MCUD12	41	ENABLE1
17	MCUD13	42	ENABLE2
18	MCUD14	43	ENABLE3
19	MCUD15	44	ENABLE4
20	MCUDPRTY	45	CB15
21	COM	46	COM
22	Т00	47	APE
23	Т01	48	SYSPE
24	T02	49	MCUDRST
25	FROMO	50	COM

NOTE: CPU/IOP Connector P2

² On pin 10 of 20-pin connector but isolated from other card cages by removal of resistor R1.

Table 1-11. IOP Bus

Table 1-12. Current Instruction Register Connector A8J1

				-				
PIN	 SIGNAL 	 PIN 	SIGNAL		PIN 	SIGNAL	 PIN 	SIGNAL
1	IODPRTY	26	IOD4	_	1		26	CIR6 Buffered
2	10X13	27	1005		2	SYSSWREGO	27	CIR7 Buffered
3		28			3	SYSSWREG1	28	PON Buffered
4	IOCMDO	29	1006		4	SYSSWREG2	29	CIR8 Buffered
5	IOCMD1	30	1007		5	SYSSWREG3	30	CIR9 Buffered
6	IOCMD1	31			6	SYSSWREG4	31	CIR10 Buffered
7		32	1008		7	SYSSWREG5	32	CIR11 Buffered
8	D E V N O O	33	IOD9		8	SYSSWREG6	33	CIR12 Buffered
9	DEVNO1	34			9	SYSSWREG7	34	CIR13 Buffered
10		35	IOD10		10		35	CIR14 Buffered
11	DEVN02	36	IOD11		11	SYSSWREG8	36	CIR15 Buffered
12	DEVNO3	37			12	SYSSWREG9	37	
13		38	IOD12		13	SYSSWREG10	38	INHAR
14	DEVNO4	39	10013		14	SYSSWREG11	39	SYSHFF
15	DEVNO5	40			15	SYSSWREG12	40	RUNFF
16		41	IOD14		16	SYSSWREG13	41	
17	DEVNO6	42	IOD15		17	SYSSWREG14	42	RUNSW
18	DEVNO7	43			18	SYSSWREG15	43	
19		44	INTREQ		19		44	LDSW
20	IODO	45	I0X12		20	CIRO Buffered	45	
21	1001	46			21	CIR1 Buffered	46	DUMPSW
22		47	IOX14		22	CIR2 Buffered	47	
23	IOD2	48	IOX15		23	CIR3 Buffered	48	IORSTSW
24	1003	49			24	CIR4 Buffered	49	
25		50	INTACK		25	CIR5 Buffered	50	CPURST

NOTE: CPU/IOP connector P3

NOTE: Connector A8J1 is cabled to the system control panel on the front door.

Table 1-13. Current Instruction Register Connector A8J2

Table 1-14. Multiplexer Channel Bus

 PIN	 SIGNAL 	 PIN 	SIGNAL		 SIGNAL 	 PIN 	SIGNAL
1		26	LDREG	1	CHANSO	26	SR10
2	PANELSWREGO	27	LDADDR	2		27	SR11
3	PANELSWREG1	28		3	SRCLOCK	28	SR12
4	PANELSWREG2	29	DISPMEM	4		29	SR13
5	PANELSWREG3	30	LDMEM	5	DEVEND	30	
6	PANELSWREG4	31		6		31	SR14
7	PANELSWREG5	32	EXECUTE	7	ACKSR	32	SR15
8	PANELSWREG6	33	SINGLE	8		33	SRO
9	PANELSWREG7	34		9	CHANACK	34	SR1
10		35	INCRADDRR	10		35	SR2
11	PANELSWREG8	36	DECADDR	11	DEVNODB	36	
12	PANELSWREG9	37		12	SIOENABLE	37	SR3
13	PANELSWREG10	38	Not used	13	EOT	38	SR4
14	PANELSWREG11	39	SYSHALTFF	14	JMPMET	39	SR5
15	PANELSWREG12	40	RUNFF	15		40	SR6
16	PANELSWREG13	41		16	TOGGLEINXFER	41	SR7
17	PANELSWREG14	42	RUNSW	17	TOGGLESR	42	
18	PANELSWREG15	43		18	TOGGLEOUTXFER	43	PCMD1
19		44	LDSW	19	TOGGLESIOOK	44	SETJMP
20	Not used	45		20		45	PSTATSTB
21	Not used	46	DUMPSW	21	XFERERROR	46	PCONTSTB
22		47		22	REQ	47	READNEXTWD
23	PSRENB	48	IORTSW	23		48	PWRITESTB
24	INHRINT	49		24	SR8	49	SETINT
25		50	CPURST	25	SR9	50	PREADSTB

NOTE: Connector A8J2 is cabled to A1J2 of the CPU card cage when using the maintenance panel.

NOTE: Multiplexer channel connector P2.

Table 1-15. Port Controller Bus

Table 1-16. Selector Channel Bus

PIN	SIGNAL	 PIN 	SIGNAL	PIN	SIGNAL	 PIN 	SIGNAL
1	ERR1	26	PCDO	1	CHANSO	 26	SR13
2	LSEL1	27	PCD1	2		27	S R1 2
3		28		3	SRCLOCK	28	S R 1 1
4	WPB	29	PCD2	4		29	SR10
5	STRB1	30	PCD3	5	DEVEND	30	
6	CWREQ1	31		6		31	S R 9
7		32	PCD4	7	ACKSR	32	SR8
8	RRREQ1	33	PCD5	8	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	33	SR7
9	T01-1	34		9	CHANACK	34	SR6
10		35	PCD6	10		35	SR5
11	T01-2	36	PCD7	11	DEVNODB	36	
12	ERR2	37		12	SIOENABLE	37	SR4
13		38	PCD8	13	EOT	38	SR3
14	LSEL2	39	PCD9	14	JMPMET	39	SR2
15	HSEL2	40		15	OHI HEI	40	SR1
16		41	PCD10	16	TOGGLEINXFER	41	SRO
17	STRB2	42	PCD11	17	CHANSR	42	310
18	CWREQ2	43		18	TOGGLEOUTXFER		DOM 0 4
19		44	PCD12	19	TOGGLESIOOK	43	PCMD1 SETJMP
20	RREQ2	45	PCD13	20	TOGGLESTOOK	4 4 4 5	PSTATSTB
21	PB14	46		21	XFERERROR	46	PCONTSTB
2.2		47	PCD14		REQ		
23	PB15	48	PCD15	22	KEU	47	READNEXTWD
24	Not used	49	_	23	SR15	48	PWRITESTB
25		50	PCDPRTY	24 25	SR14	49 50	SETINT

NOTE: Selector channel connector P2

Table 1-17. Selector Channel Connector J1

Table 1-18. Selector Channel Connector J2

PIN	SIGNAL	 PIN	SIGNAL		PIN	SIGNAL	 PIN	SIGNAL
1 2 17	OIGHAL		OIGHAL		PIN	SIGNAL		SIGNAL
				•	'			
1	FREEZE	26	LDBANK		1	FSENB	26	RBB2
2	RESET	27			2	TRBENB	27	
3		28	RRREQ		3		28 29	RBB1
4	WPB	29	WBA1		4	LA	29	ENDB
5	WBB2	30			5	IOPCNTDN	30	
6		31	WAIT		6		31	DEVNOADR
7	WBA2	32	XERR		7	DPE	32	IOAWADR
8	SENSEACK	33	XENN		8	DATA	33	IOAWADK
9		34	WBB1		9	VA 1 A	34	RBA2
10	CW1	35	CWREQ		10	WCTC	35	CW2
11	TRB1FF	36			11	IOCW4	36	
12		37	IOPCNTDATA		12		37	RPB
13	JUMPFF	38	DATAINACK		13	IOCWO	38	HSEL
14	CHACTIVE	39			14	IOCW1	39	
15		40	RRDATA		15		40	LDRR
16	TRB2FF	41	PCRST		16	IOCW2	41	STRB
17	AWBWAIT	42			17	100W2	42	STRE
1.8	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	43	IOPCNTWAIT		18	100#3	43	LSEL
18 19	CWBWAIT	44	PFSENB		19	WFRTC	44	WCRO
20	WT	45			20	INTCLRIL	4 5	# 5 K 5
						_ _ _	• •	
21		46	INCWC		21		46	PCERR
22	DATAOUT	47	ADR		22	RBA1	47	ILLADR
23	IOCWWAIT	48			23	LDDEVNO	48	
24		49	DATAOUTACK		24		49	RESREQ
25	IOAWWAIT	50	GOACTIVE		25	IOPCNTADR	50	KEND

Table 1-19. Memory Connector J1

 PIN	 Signal 	 PIN 	SIGNAL
1		26	DATA6
2	Not used	27	
3		28	DATA7
4	Not used	29	
5		30	DATA8
6	Not used	31	
7		32	DATA9
8	Not used	33	
9		34	DATA10
10	Not used	35	
11		36	WRITE
12	Not used	37	
13		38	READ
14	DATAO	39	
15		40	RFSH
16	DATA1	41	
17		42	RAS
18	DATA2	43	
19		44	ROW2
20	DATA3	45	
21		46	ROW1
22	DATA4	47	
23		48	ROWO
24	DATA5	49	
25		50	CAS

Table 1-20. Memory Connector J3

1 26 BDO 27 28 DATA11 29 DATA12 6 MAO 31 TATA 13 TATA 14 DATA14 TATA 15 TATA 16 MAS TATA 16 MAS TATA 17 TATA 1	 PIN	 SIGNAL 	 PIN 	SIGNAL
4 Not used 29 30 DATA12 6 MAO 31 7 32 DATA13 8 MA1 33 9 34 DATA14 10 MA2 35 11 36 DATA15 12 MA3 37 13 38 CO 14 MA4 39 15 40 C1 16 MA5 41 17 42 C2 18 MA6 43 19 C1 18 MA6 43 19 C2 10 Not used 45 21 DISWEC 47 23 24 BD1 49	1			BDO
4 Not used 29 30 DATA12 6 MAO 31 7 32 DATA13 8 MA1 33 9 34 DATA14 10 MA2 35 11 36 DATA15 12 MA3 37 13 38 CO 14 MA4 39 15 40 C1 16 MA5 41 17 42 C2 18 MA6 43 19 C1 18 MA6 43 19 C2 10 Not used 45 21 DISWEC 47 23 24 BD1 49	2	Not used		
5 30 DATA12 6 MAO 31 7 32 DATA13 8 MA1 33 9 34 DATA14 10 MA2 35 11 36 DATA15 12 MA3 37 13 38 CO 14 MA4 39 15 40 C1 16 MA5 41 17 42 C2 18 MA6 43 19 C3 20 Not used 45 21 DISWEC 47 23 24 BD1 49	3			DATA11
6 MAO 31 7 32 DATA13 8 MA1 33 9 34 DATA14 10 MA2 35 11 36 DATA15 12 MA3 37 13 38 CO 14 MA4 39 15 40 C1 16 MA5 41 17 42 C2 18 MA6 43 19 A4 C3 20 Not used 45 21 22 DISWEC 47 23 24 BD1 49	4	Not used		
32 DATA13 8 MA1 33 9 34 DATA14 10 MA2 35 11 36 DATA15 12 MA3 37 13 38 CO 14 MA4 39 15 40 C1 16 MA5 41 17 42 C2 18 MA6 43 19 44 C3 20 Not used 45 21 22 DISWEC 47 23 24 BD1 49	5		30	DATA12
8 MA1 33 34 DATA14 10 MA2 35 DATA14 11 36 DATA15 12 MA3 37 13 38 CO 314 MA4 39 15 40 C1 16 MA5 41 17 42 C2 18 MA6 43 19 44 C3 20 Not used 45 C5 21 DISWEC 47 23 24 BD1 49 C5	6	MAO		
9 10 MA2 35 DATA14 11 36 DATA15 12 MA3 37 13 38 CO 14 MA4 39 15 40 C1 16 MA5 41 17 42 C2 18 MA6 43 19 C0 Not used 44 C3 20 Not used 45 21 22 DISWEC 47 23 24 BD1 48 C5				DATA13
10 MA2 35 11 36 DATA15 12 MA3 37 13 38 CO 14 MA4 39 15 40 C1 16 MA5 41 17 42 C2 18 MA6 43 19 44 C3 20 Not used 45 21 22 DISWEC 47 23 24 BD1 49		MA1		
11				DATA14
12 MA3 37 13 38 C0 14 MA4 39 15 40 C1 16 MA5 41 42 C2 18 MA6 43 44 C3 20 Not used 45 21 22 DISWEC 47 23 24 BD1 49	10	MA2	35	
13 14 MA4 39 15 40 C1 16 MA5 41 42 C2 18 MA6 43 19 20 Not used 46 C4 22 DISWEC 47 23 24 BD1 38 C0 38 C0 40 C1	11			DATA15
14 MA4 39 15 40 C1 16 MA5 41 17 42 C2 18 MA6 43 19 44 C3 20 Not used 45 21 46 C4 22 DISWEC 47 23 48 C5 24 BD1	12	MA3		
15 40 C1 16 MA5 41 17 42 C2 18 MA6 43 19 44 C3 20 Not used 45 21 46 C4 22 DISWEC 47 23 48 C5 24 BD1 49	13			CO
16 MA5 41 17 42 C2 18 MA6 43 19 44 C3 20 Not used 45 21 46 C4 22 DISWEC 47 23 48 C5 24 BD1 49	14	M A 4		
17	15		40	C1
18 MA6 43 19 44 C3 20 Not used 45 21 46 C4 22 DISWEC 47 23 48 C5 24 BD1 49	16	MA5	41	
19	17			C2
20 Not used 45 21	18	MA6		
21 46 C4 22 DISWEC 47 23 48 C5 24 BD1 49	19			C3
22 DISWEC 47 23 48 C5 24 BD1 49	20	Not used	45	
23 48 C5 24 BD1 49	21			C 4
24 BD1 49	22	DISWEC		
- · · · · · · · · · · · · · · · · · · ·	23			C 5
25 50 Not used		BD1		
			50	Not used

Table 1-21. Error Logging Interface Cable

 PIN	 SIGNAL 	 PIN 	SIGNAL
1 2	DISWEC	26 27	ELAD7
2 3 4	Not used	28 29	ELAD6
5	SELECT	30	
6 7	L∕ u imb	31 32	ELAD5
8 9	PRESET	33 34	ELAD4
10	PRESEI	35	ELADO
11 12	Not used	36 37	ELAD1
13 14	ELDS	38 39	ELAD2
15	ELAV	40	
16 17	SELECTED	41 42	ELAD3
18		43	DATA IN
19 20	ELAW	44 45	Not used
21	ELAD8	46 47	Not used
22 23	ELAD9	48 49	Not used
24 25	DATAOUT	50	NOL USEU

Table 1-22. IOP Power Bus (Memory Card Cage)

PIN N	UMBER	SIGNAL	PIN N	UMBER	SIGNAL
56-PIN	20-PIN		56-PIN	20-PIN	
1		+5V	30		EVD
2		+5 V	31		-5VB
3		+5 V	32 33		-5VB
4 5	2	+5V PFWARN	34		
6	1	ENTIMER	35		+5 VB
7	4	Not used	36		+5VB
8	3	Not used	37		+12VB
9	6	PWRON	38		+12VB
10	5	PWRON	39		+12.7VB
11 -	8	IORESET	40		+12.7VB
12	7	IORESET	41	12	Not used
13	10	MCUCLK	42	11	Not used
14	9	MCUCLK	43		Not used
15			44		Not used
16			45		Not used
17		Not used	46	13	Not used
18		Not used	47		Not used
19			48		Not used
20			49	16	SI
21			50	15	SI
22			51		MCUFRCOUT
23		Not used	52		MCUFRCOUT
24		Not used	53	18	S 0
25		Not used	54	17	S 0
26		Not used	55		MCUFRCIN
27		Not used	56		MCUFRCIN
28		Not used		20	Not used
29				19	Not used

Table 1-23. Mag Tape Interface Connector J2

Table 1-24. Mag Tape Interface Connector J3

PIN	SIGNAL	 PIN 	SIGNAL		PIN	SIGNAL	 PIN 	SIGNAL
1		26	Not used	•	1		26	FLG5
2		27	ROM16		2	CLEAR	27	FLG2
3	ROM4	28	ROMO		3	TO T3 T2	28	FLG3
4	Not used	29	ROM17		4	<u>T3</u>	29	FLGO
5	ROM5	30	ROM1		5	TŽ	30	FLG1
6	Not used	31	ROM18		6	ROR9	31	Not used
7	ROM6	32	ROM2		7	UDS	32	EXTSEL
8	Not used	33	ROM19		8	INPUT STROBE	33	Not used
9	ROM7	34	ROM3		9	FLG10	34	Not used
10	Not used	35	Not used		10	LOS	35	Not used
11	ROM8	36	Not used		11	FLG14	36	Not used
12	Not used	37	RARO		12	FLG12	37	Not used
13	ROM9	38	RAR1		13	FLG16	38	Not used
14	Not used	39	RAR2		14	FLG15	39	T1
15	ROM10	40	RAR3		15	ROR8	40	Not used
16	Not used	41	RAR4		16	FLG17	41	Not used
17	ROM11	42	RAR5		17	ROR11	42	Not used
18	Not used	43	RAR6		18	ROR7	43	Not used
19	ROM12	44	RAR7		19	WT1	44	Not used
20	Not used	45	RAR8		20	ROR10	45	Not used
21	ROM13	46	RAR9		21	FLG13	46	Not used
22	Not used	47	RAR10		22	FLG11	47	Not used
23	ROM14	48	RAR11		23	FLG6	48	Not used
24	Not used	49			24	FLG7	49	Not used
25	ROM15	50			25	FLG4	50	

Table 1-25. Mag Tape Interface to Tape Unit

Table 1-26. 7920A/7925A Disc Interface to Device Controller

 PIN	SIGNAL	 PIN 	SIGNAL	PIN	SIGNAL	 PIN 	SIGNAL
1	Not used	26	Not used	1	+5V	26	Not used
2	SING TRK ERR	27	Not used	2	+5V	27	IBUS3
3	SELECT CMD O	28	Not used	3	IFNO	28	CLEAR
4	SELECT CMD 1	29	ID BURST	4	IFN2	29	ENID
5	SELECT CMD 2	30	WRCLK	5	IFN1	30	Not used
6	SELECT CMD 3	31	MULT TRK ERR	6	IFN3	31	IFCLK
7	END OF BLOCK	32	TAPE MARK	7	FLG3	32	Not used
8	READ CLK	33	WRITE DATA O	8	IBUS4	33	
9	READ DATA PRTY	34	WRITE DATE 1	9	FLGO	34	
10	WRT DATA PRTY	35	WRITE DATA 6	10	IBUS5	35	+5V
11	WRITE RESET	36	WRITE DATA 7	11	FLG6	36	+5V
12	STAT 800/1600	37	WRITE DATA 4	12	IBUS6	37	IBUS8
13	LOAD POINT	38	WRITE DATA 5	13	IFNVALID	38	IBUS12
14	READY	39	WRITE DATA 2	14	IBUS7	39	IBUS 9
15	FILE PROTECT	40	WRITE DATA 3	15		40	IBUS13
16	END OF TAPE	41	READ DATA 6	16		41	IBUS10
17	FORWARD	42	READ DATA 7	17	Not used	42	IBUS14
18	REVERSE	43	READ DATA 4	18	POWERFAIL	43	IBUS11
19	WRITE	44	READ DATA 5	19		44	IBUS15
20	OFF LINE	45	READ DATA 2	20		45	Not used
21	REWIND	46	READ DATA 3	21	IBUSO	46	FLG7
22	WRRST	47	READ DATA O	22	+5V	47	FLG1
23	Not used	48	READ DATA 1	23	IBUS1	48	FLG8
24	Not used	49	Not used	24	Not used	49	
25	Not used	50	Not used	25	ĪBUS2	50	

Table 1-27. 7920A/7925A Disc Controller Connector J2

Table 1-28. 7920A/7925A Disc Controller Connector P2

PIN	SIGNAL		SIGNAL		SIGNAL	 PIN	SIGNAL
 1		26	ROMO	1		26	EXTFLG5
2		27	ROM1	2	CLEAR	27	EXTFLG2 (EOW)
3	ROM19	28	Not used	3	CYCLECLK	28	EXTFLG3
4	ROM18	29	RAR2	4	Not used	29	EXTFLGO
5	ROM7	30	Not used	5	EXTFLG16	30	EXTFLG1
6	ROM6	31	RAR1	6	XADDR2	31	M12
7	ROM5	32	Not used	7	UBOUT	32	EXTSEL
8	ROM4	33	RARO	8	INPUT	33	M13
9	ROM17	34	Not used	9	EXTFLG8	34	M13 M11
10	ROM16	35	ROM15	10	LBOUT	35	M14
11	ROM8	36	Not used	11	EXTFLG12	36	M10
12	ROM9	37	ROM14	12	EXTFLG10	37	M15
13	ROM10	38	Not used	13	EXTFLG14	38	M9
14	Not used	39	ROM13	14	EXTFLG13	39	TESTCLK
15	ROM11	40	Not used	15	XADDR3	40	<u>m8</u>
16	Not used	41	ROM12	16	EXTFLG15	41	M3
17	RAR7	42	ROM23	17	XADDRO	42	M4
18	Not used	43	ROM22	18	XADDR4	43	<u>M2</u>
19	RAR6	44	Not used	19	CLKDISABLE	44	M 5
20	Not used	45	ROM21	20	XADDR1	45	M3 M4 M2 M5 M1
21	RAR5	46	Not used	21	EXTFLG11	46	<u>M6</u>
22	RAR4	47	ROM20	22	EXTFL G9		M6 M0
23	RAR3	48	Not used	23	EXTFLG6	48	<u>M7</u>
24	ROM2	49		24	EXTFLG7	49	Not used
25	ROM3	50		25	EXTFLG4	50	

Table 1-29. 7920A/7925A Disc Controller Connector P3

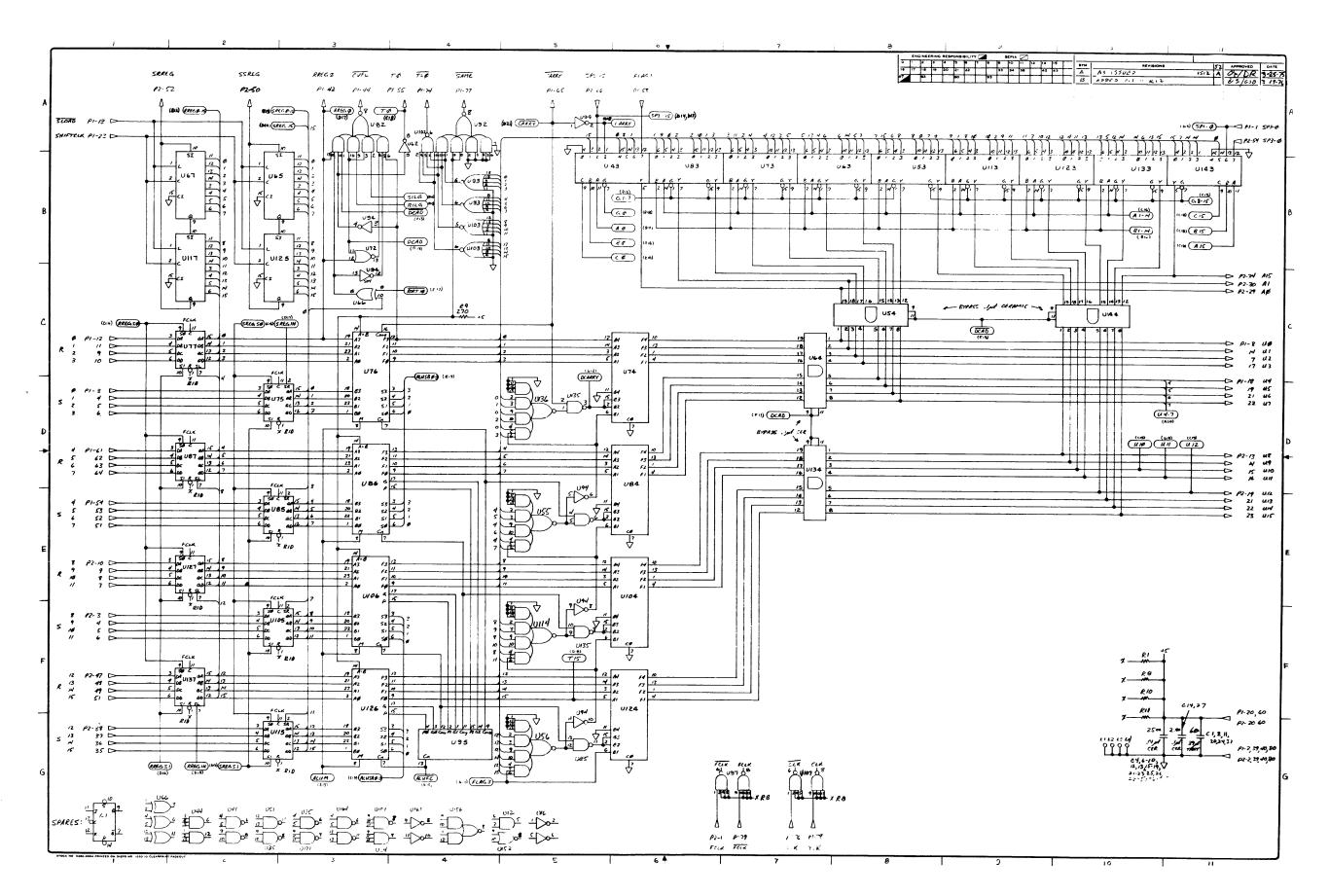
Table 1-30. Disc Controller to 7920A/7925A Disc Drive

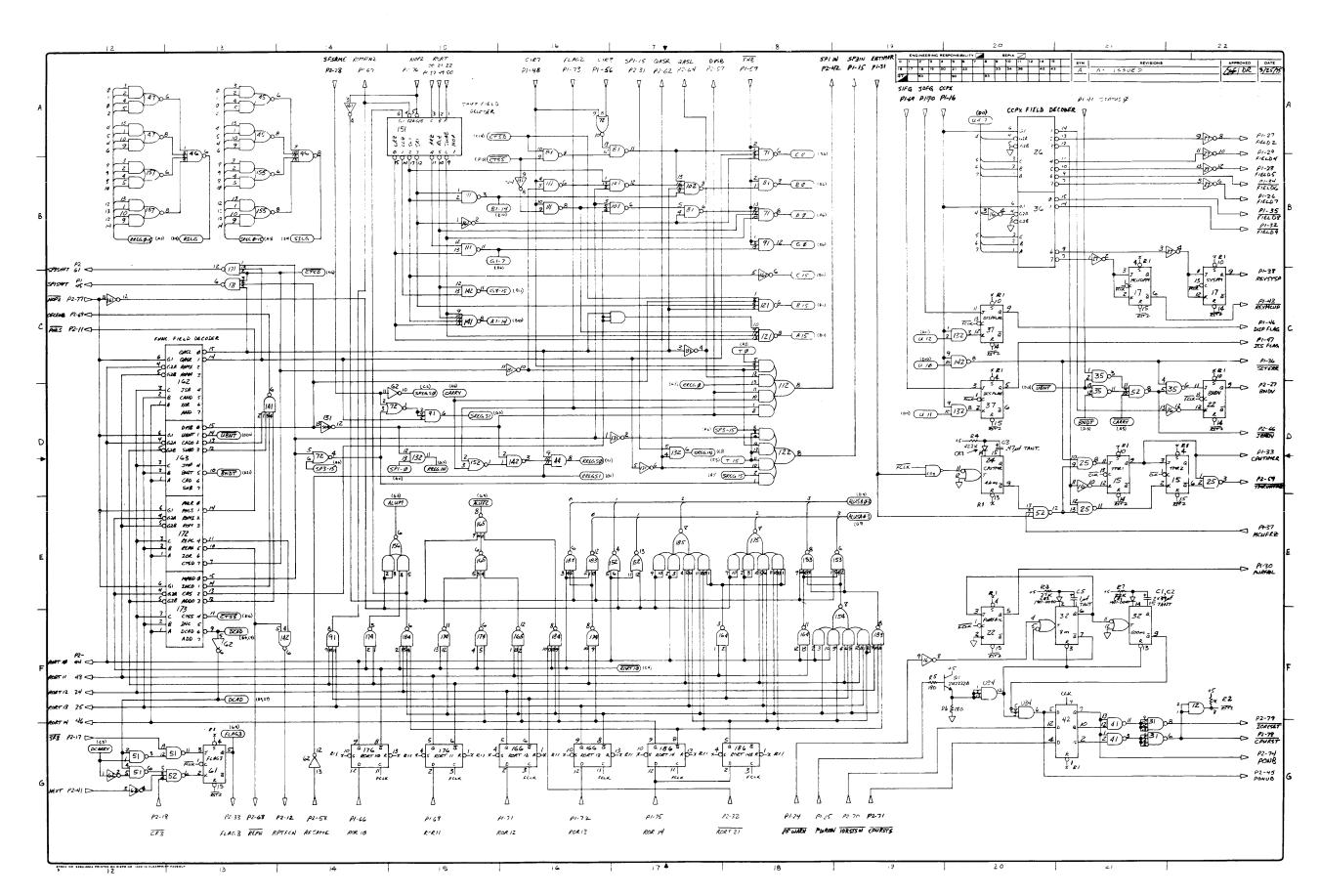
PIN	SIGNAL	 PIN 	SIGNAL	PIN	SIGNAL	 PIN 	SIGNAL
1		26	READ NRZ DATA	1	+5V	26	Not used
2	30MHZ	27		2	+5V	27	CBUS7
3		28	Not used	3	CBUSO	28	Not used
4	+5V	29		4	CBUS11	29	
5		30	Not used	5	CBUS1	30	Not used
6	INHCRCCLK	31		6	CBUS10	31	
7		32	DATACLK	7	CBUS2	32	Not used
8	Not used	33		8	CBUS9	33	
9		34	TESTCLR	9	CBUS3	34 35	
10	WRITEDATATEST	35		10	CBUS8	35	+5V
11		36	SYNC	11		36	+5 V
12	WRITECLK	37		12		37	Not used
13	WILLIEGER	38	TEST OUTPUT	13	Not used	38	CBUS12
14	WRITETEST	39	, 20, 00, 00	14		39	Not used
15	***************************************	40	Not used	15		40	CBUS13
16	+5V	41		16		41	Not used
17		42	Not used	17	Not used	42	CBUS14
18	+5V	43		18	Not used	43	Not used
19	. 5 🗸	44	ECCSERIALDATA	19		44	CBUS15
20	Not used	45		20		45	
21		46	Not used	21	CBUS4	46	
22	READTEST	47		22	+5V	47	
23	KEND I EO I	48	Not used	23	CBUS5	48	
24	READCLK	49		24	Not used	49	
25	KENVCEK	50	CLOCKINHIBIT	25	CBUS6	50	

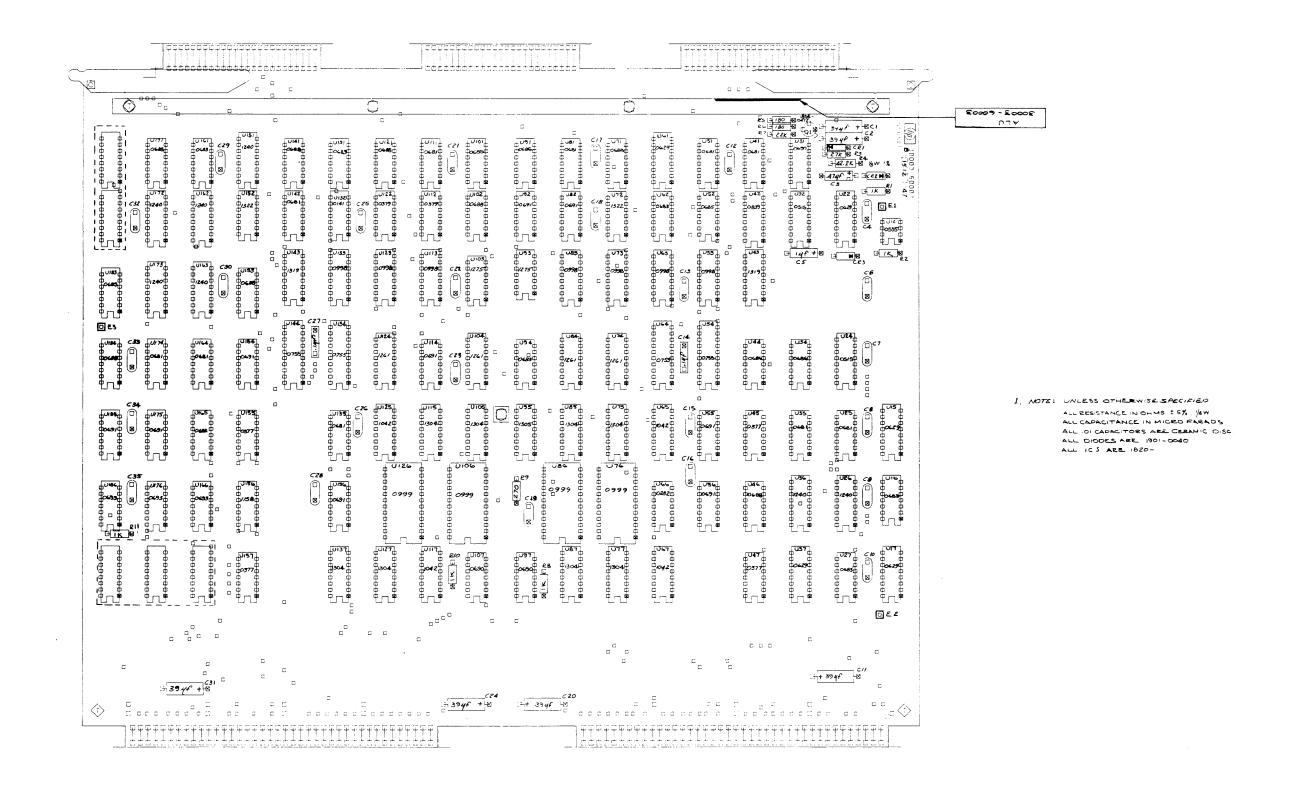
SECTION II - CPU AND MEMORY PCAS

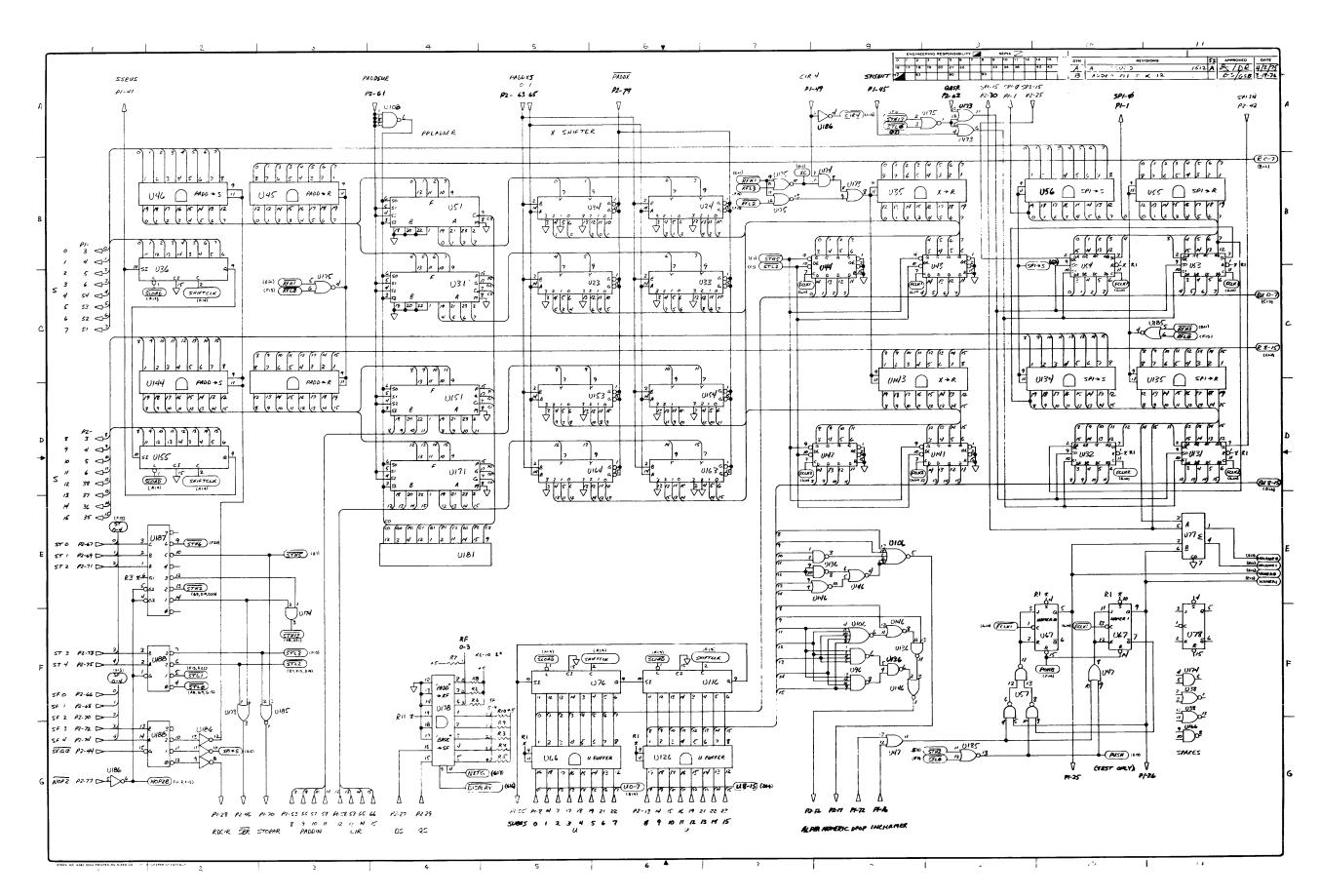
CONTENTS

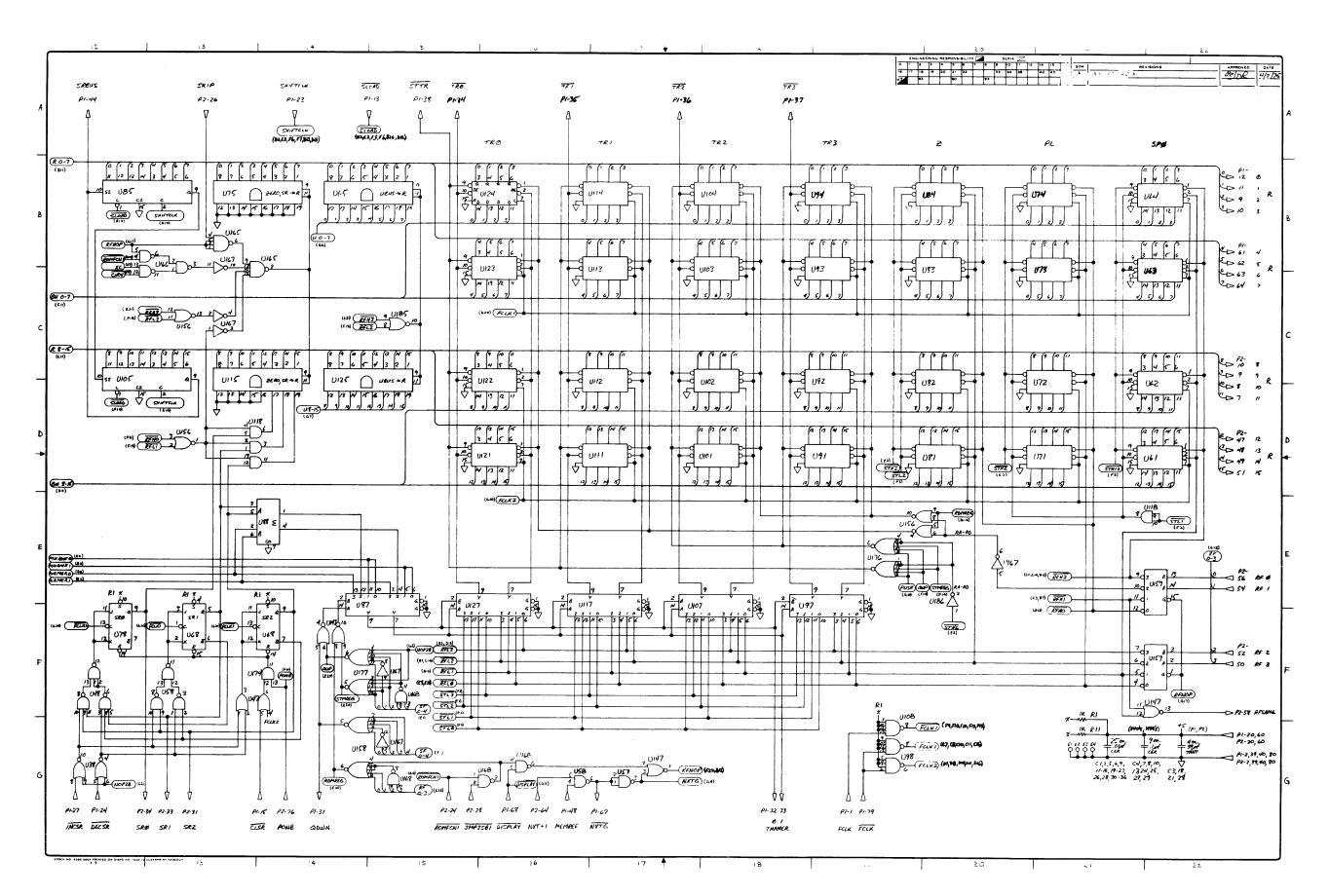
PCA NO.	ME
30003-60003	US
30003-60007	CU OM
30003-60025	US OP
30008-60003	MA LI

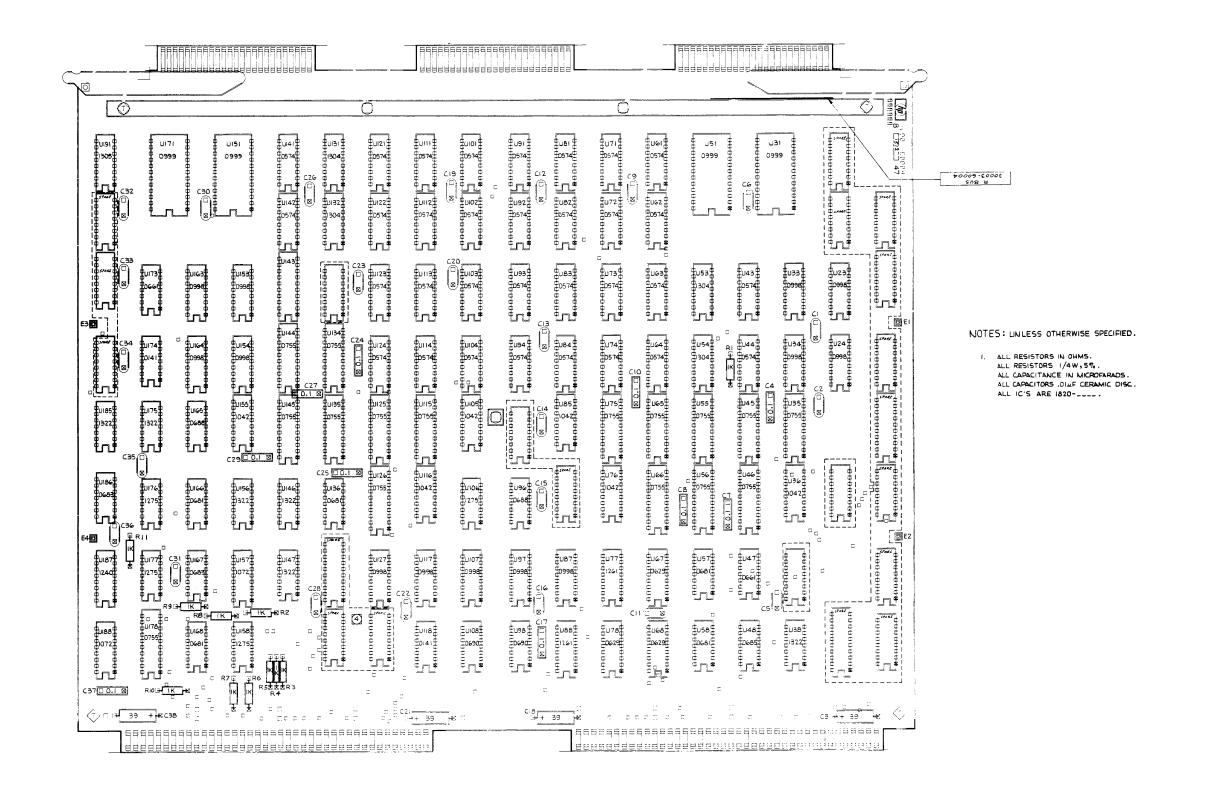


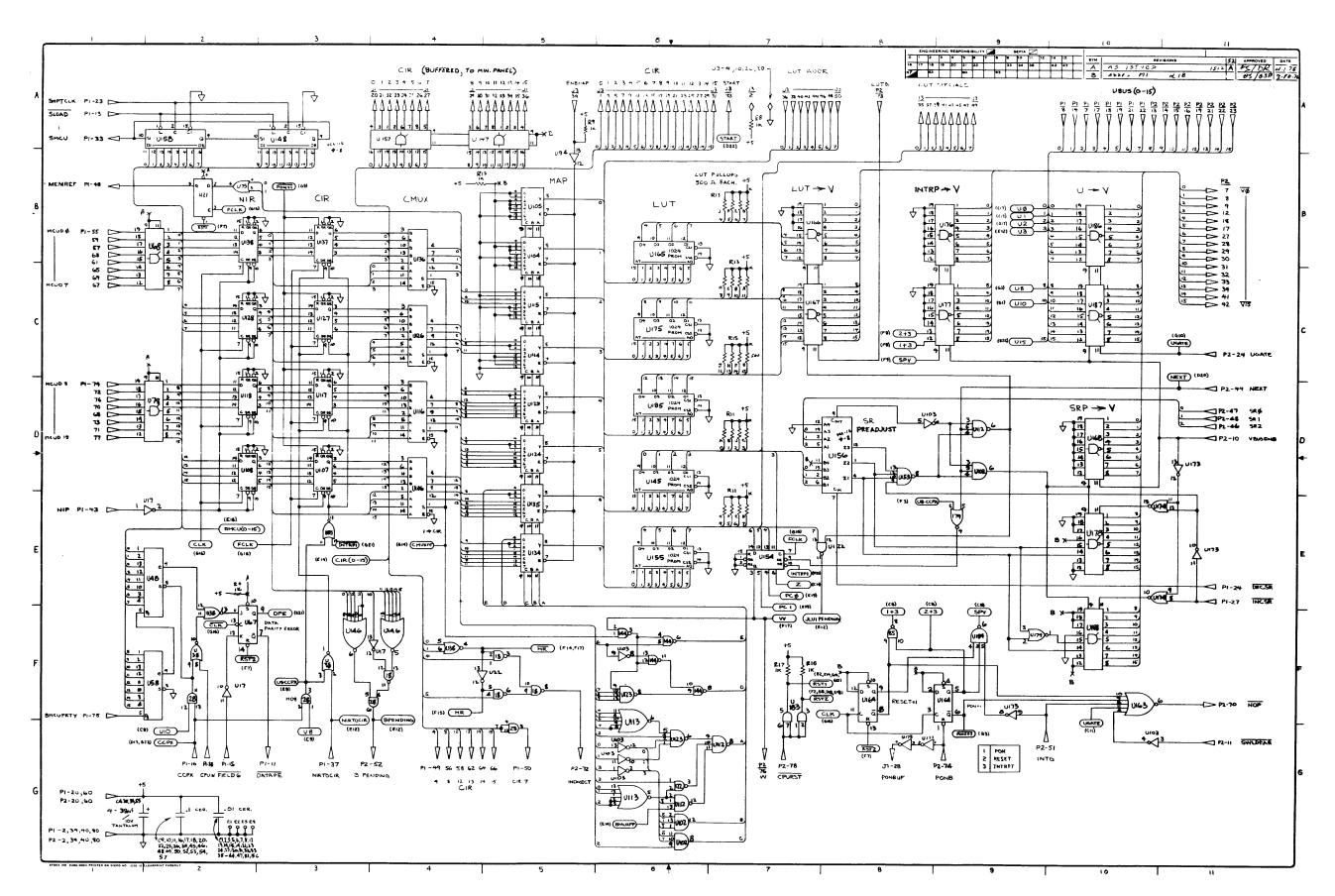


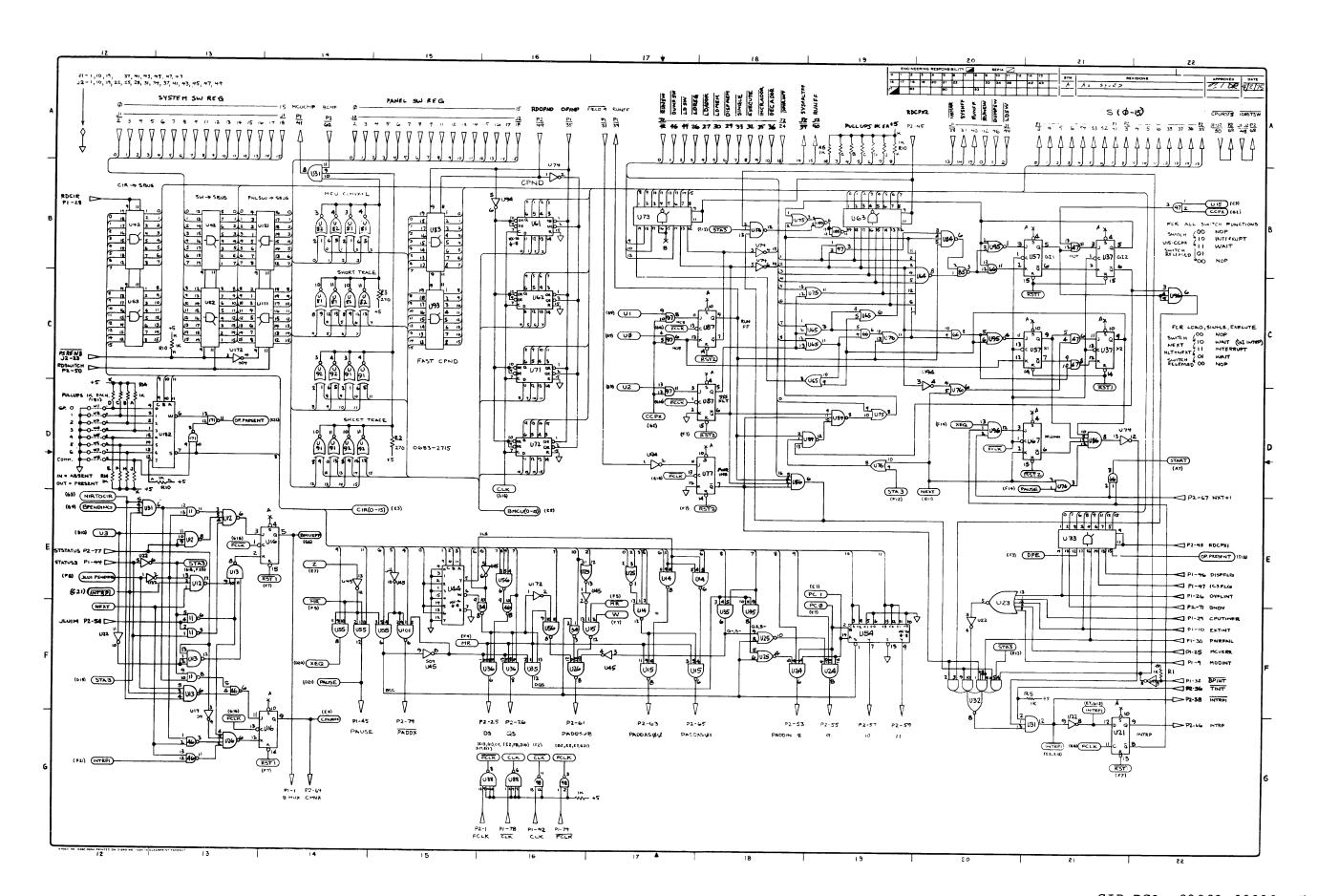


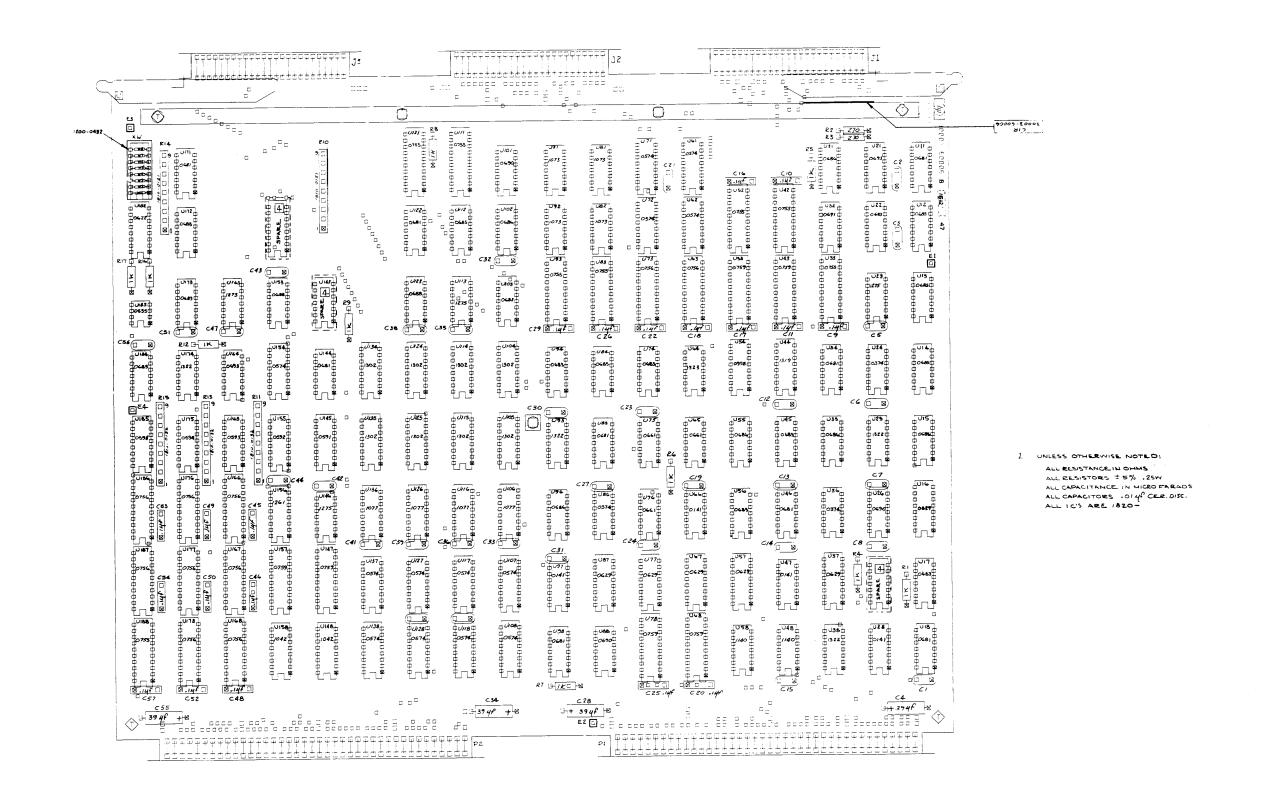


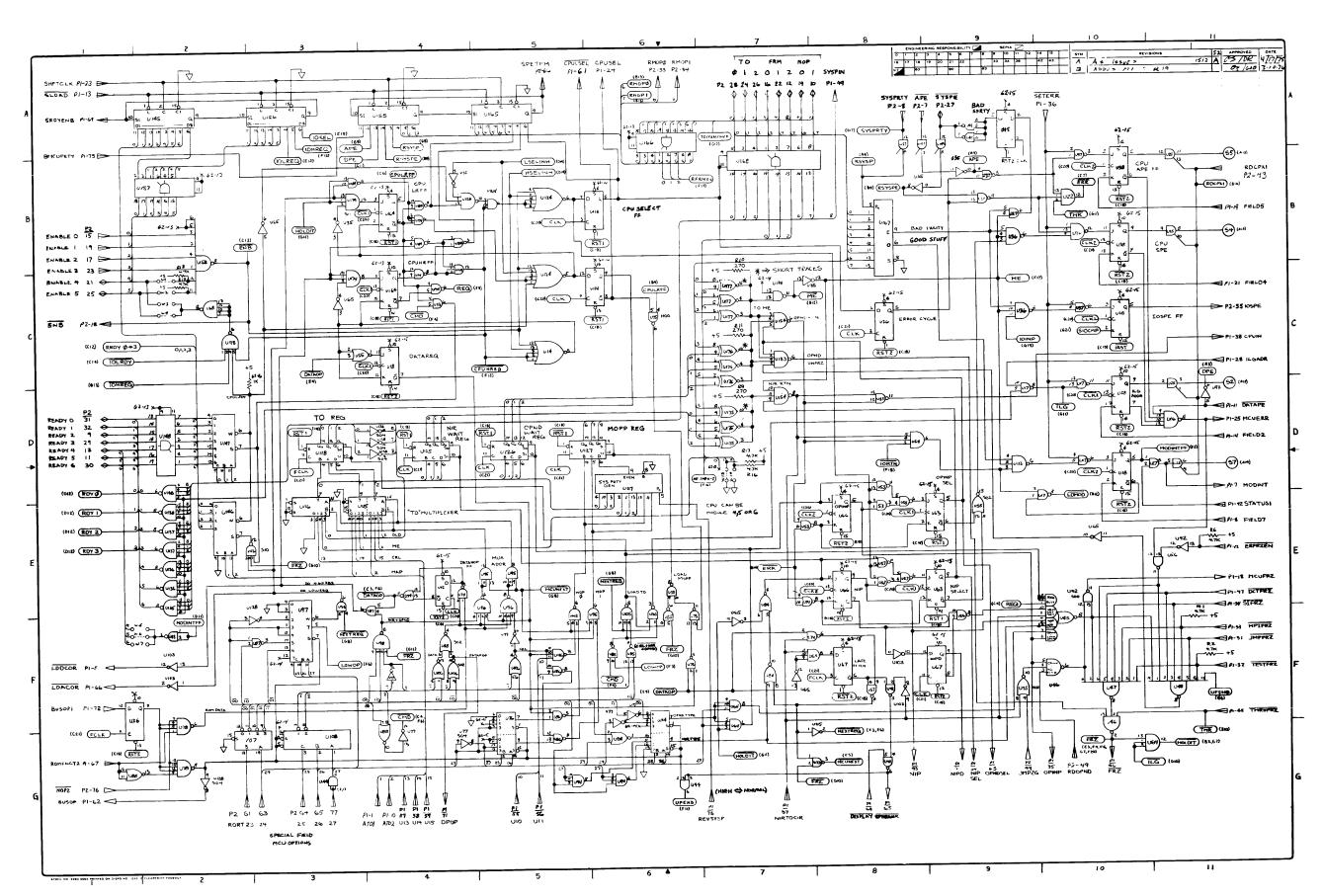


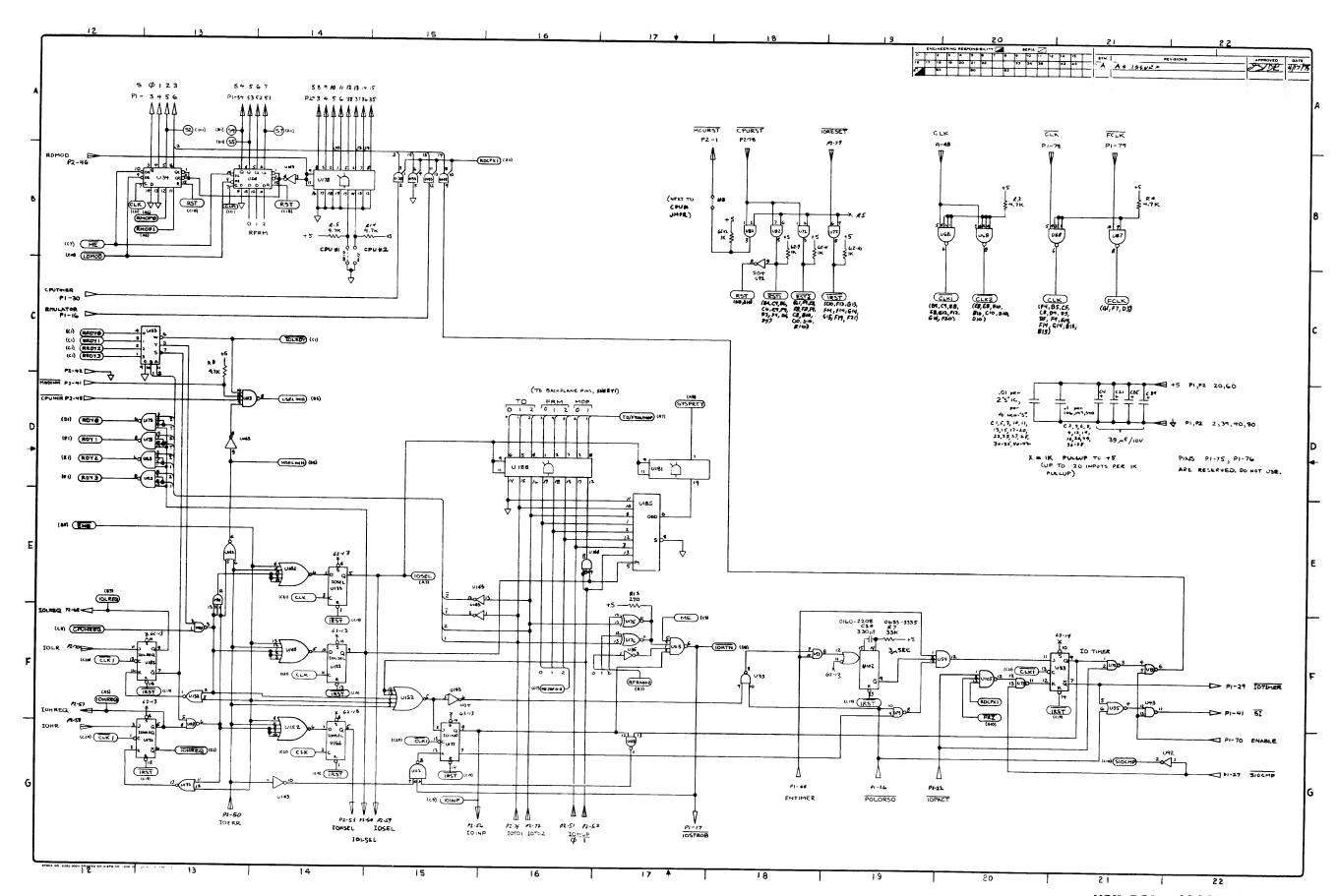


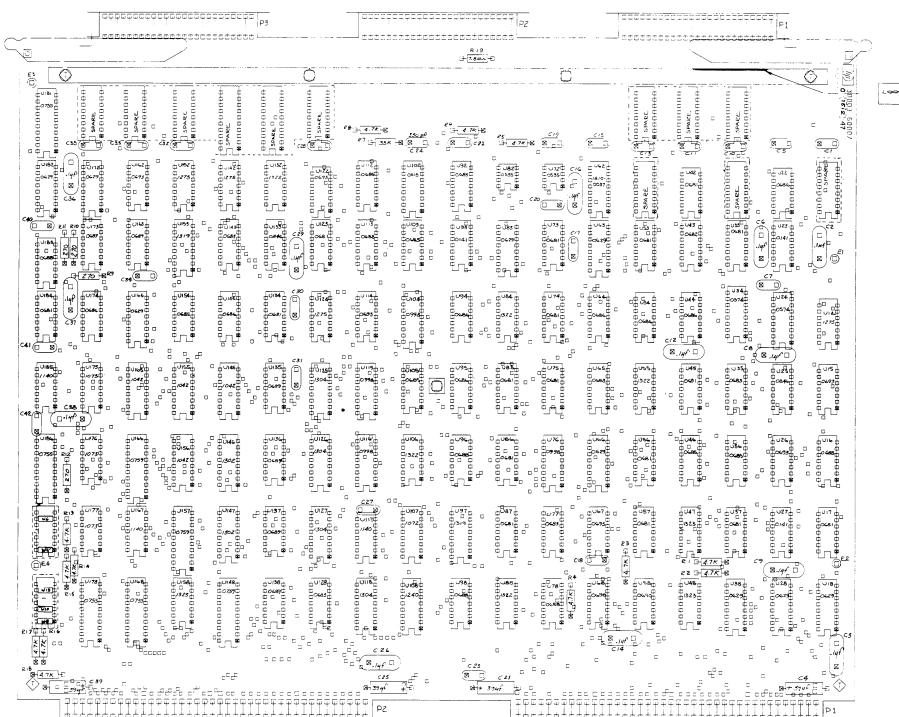












U D M F 00005

1. NOTE:

OTE:

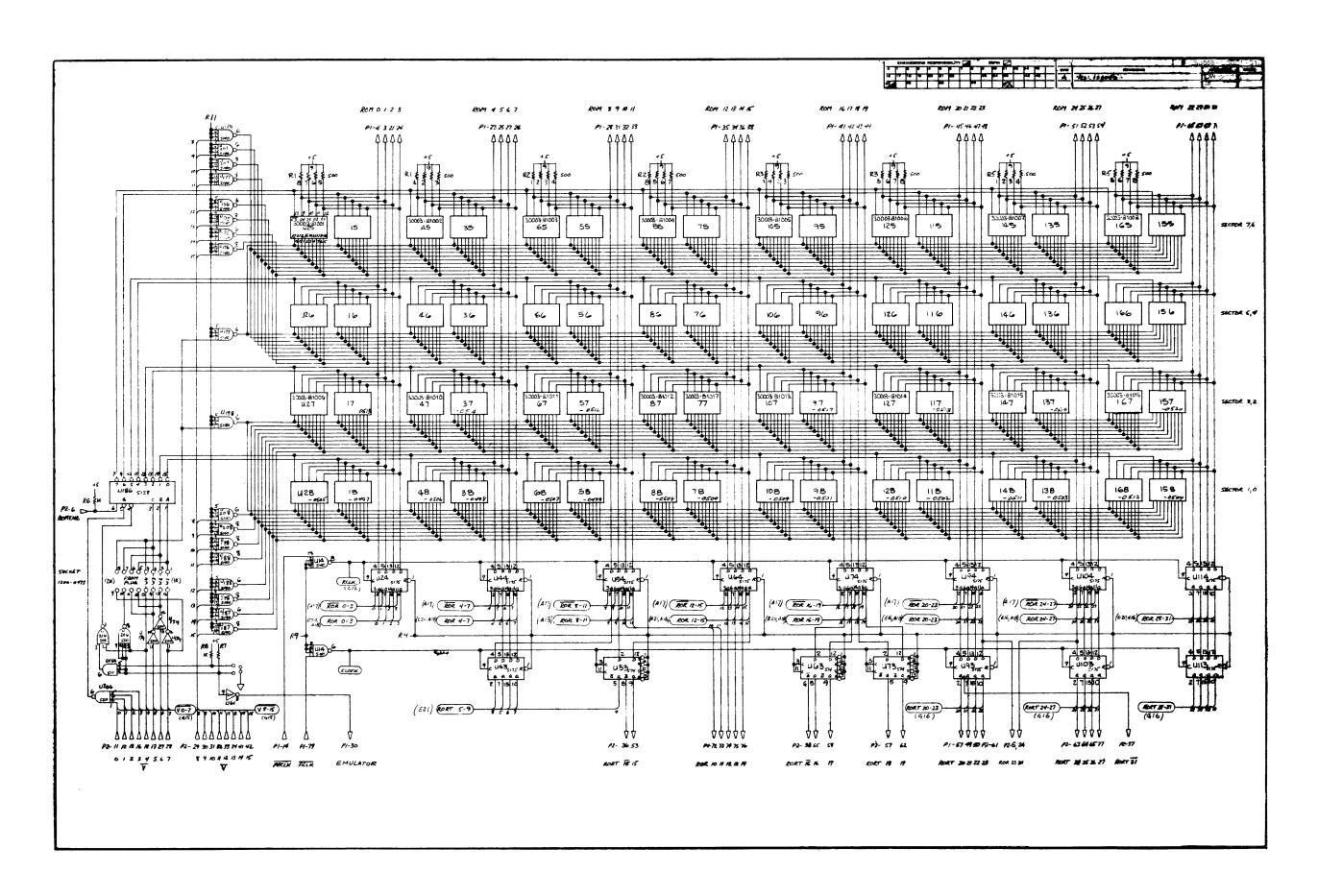
UNLESS OTHERWISC SPECIFIED:

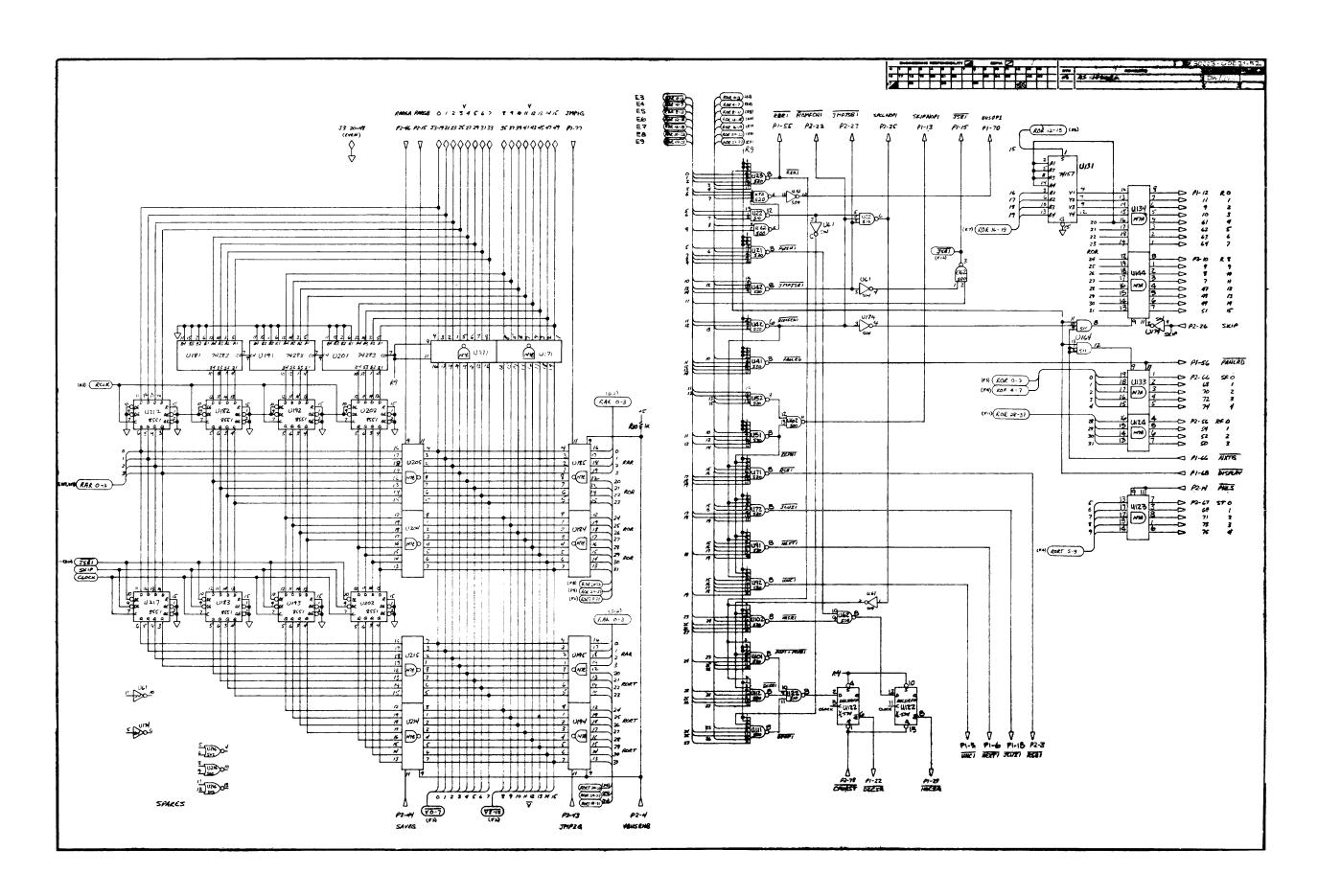
ALL RESISTANCE IN OHMS

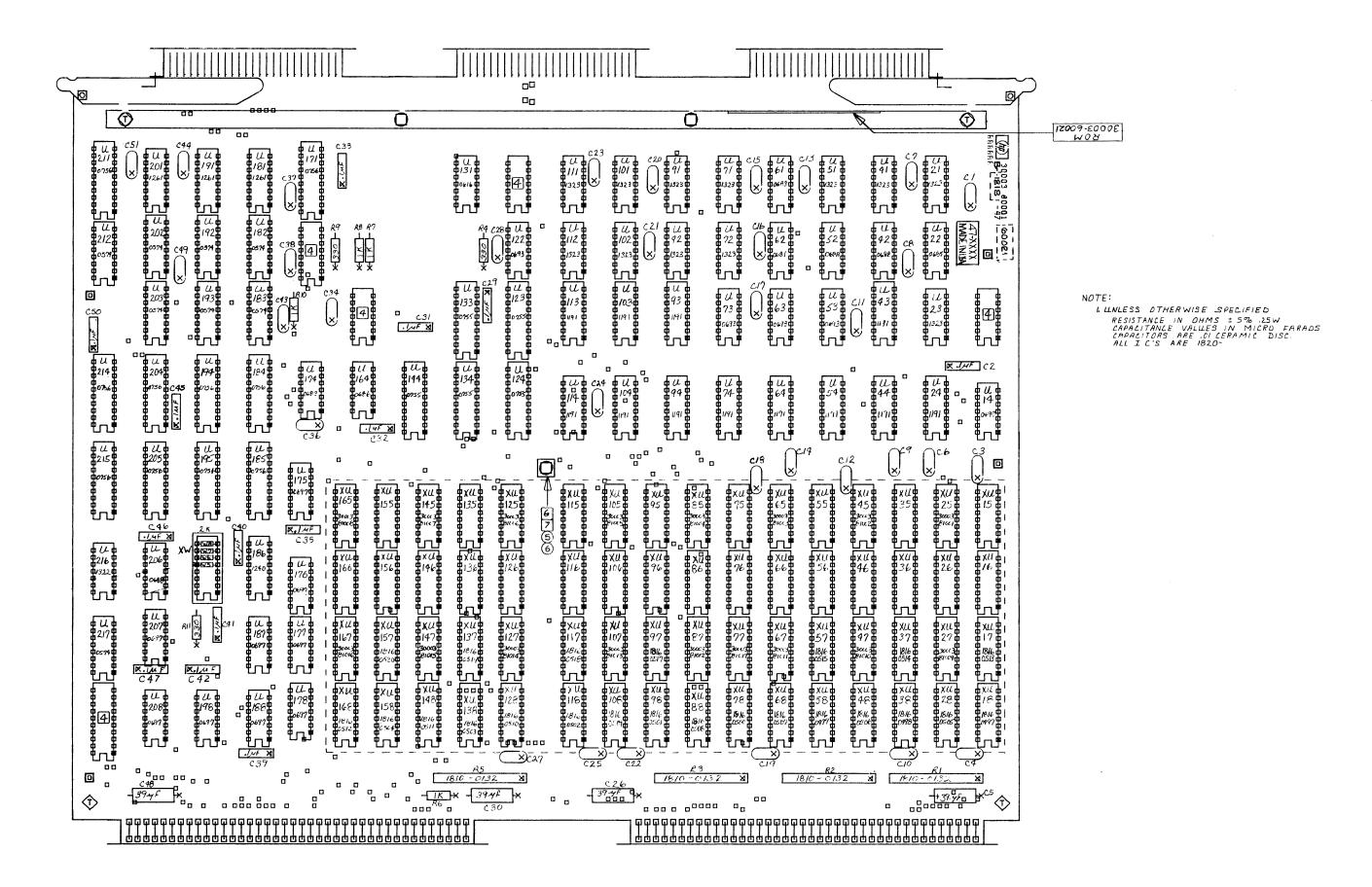
ALL RESISTORS ARE 14W 5%

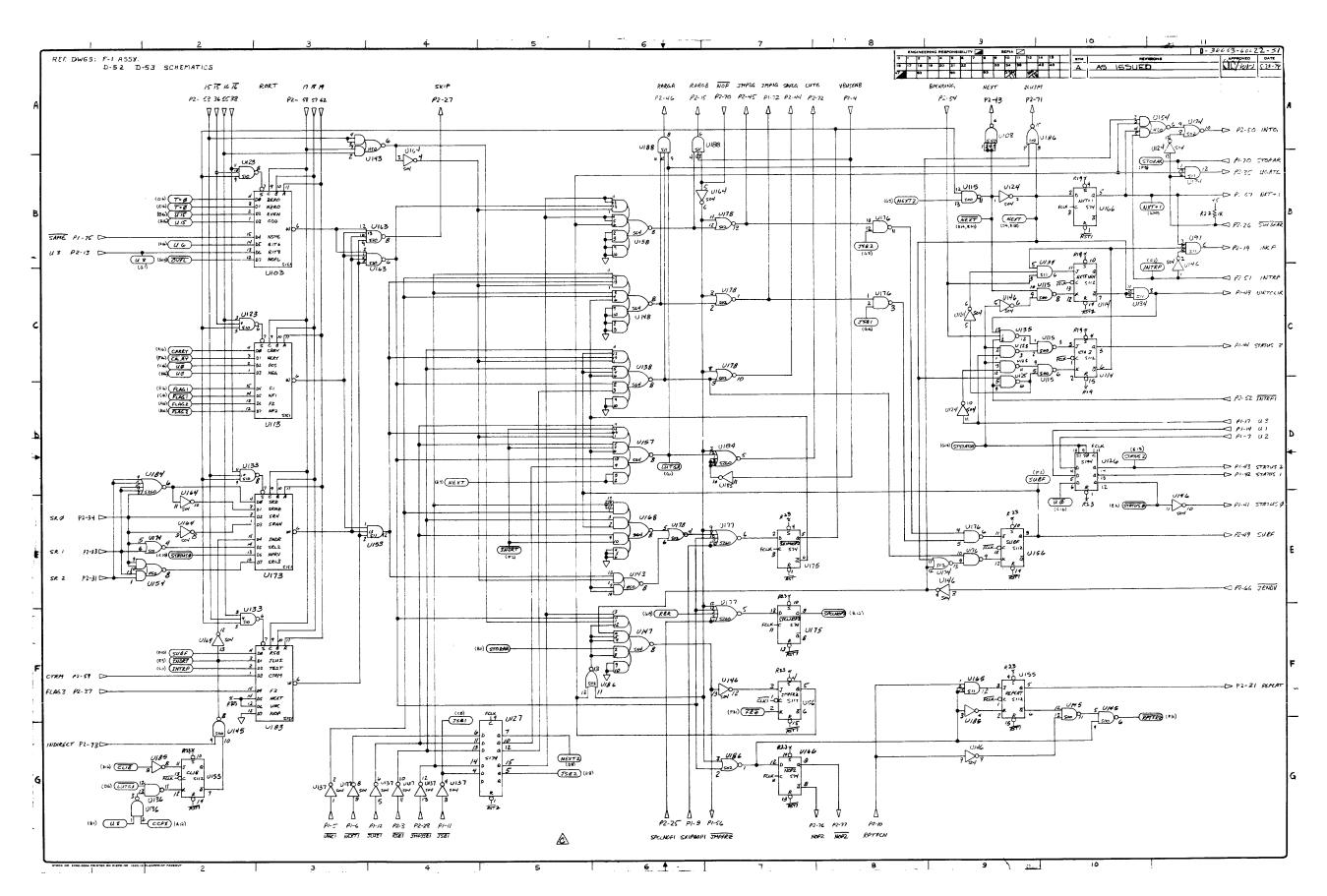
ALL CAPACITANCE IN MICRO FARADS

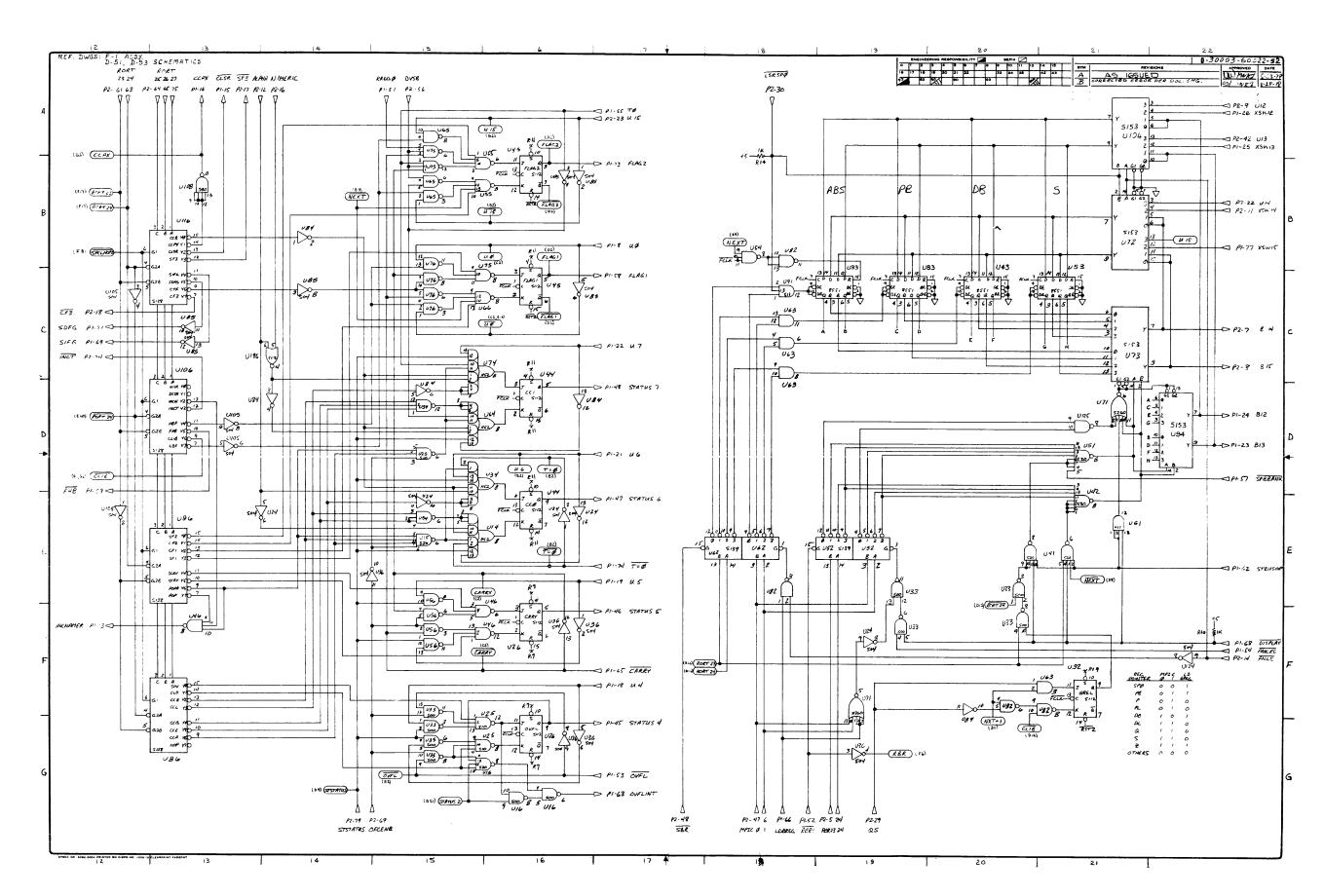
ALL CAPACITORS ARE 01. 0160-2055

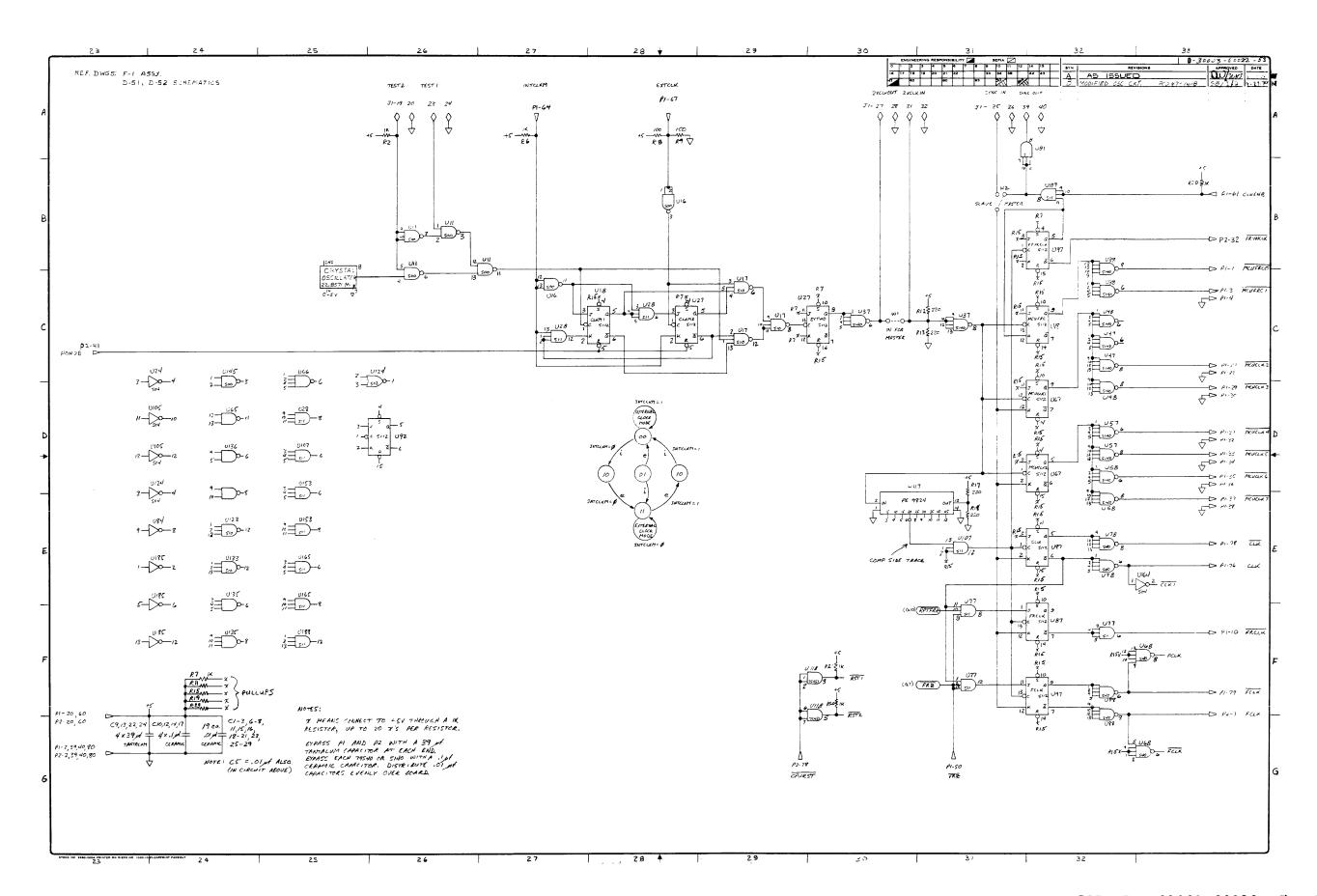


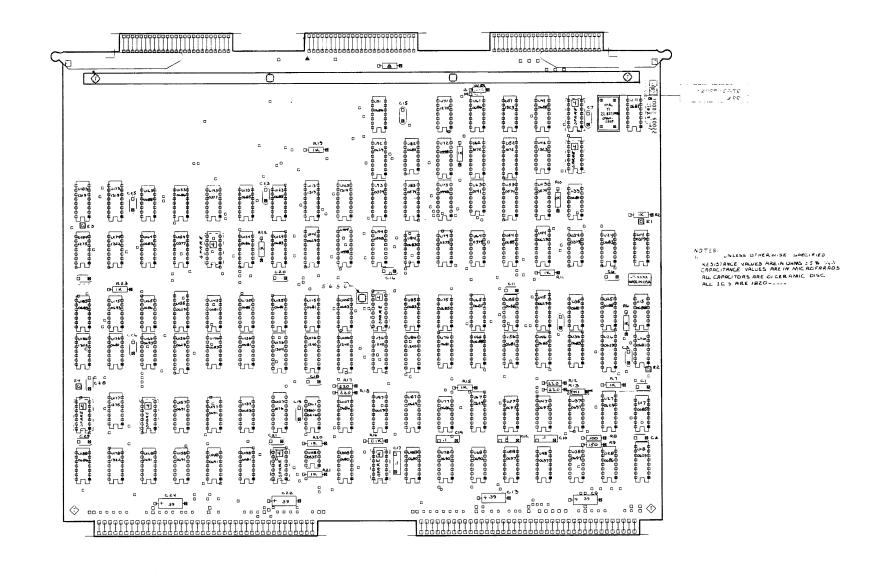


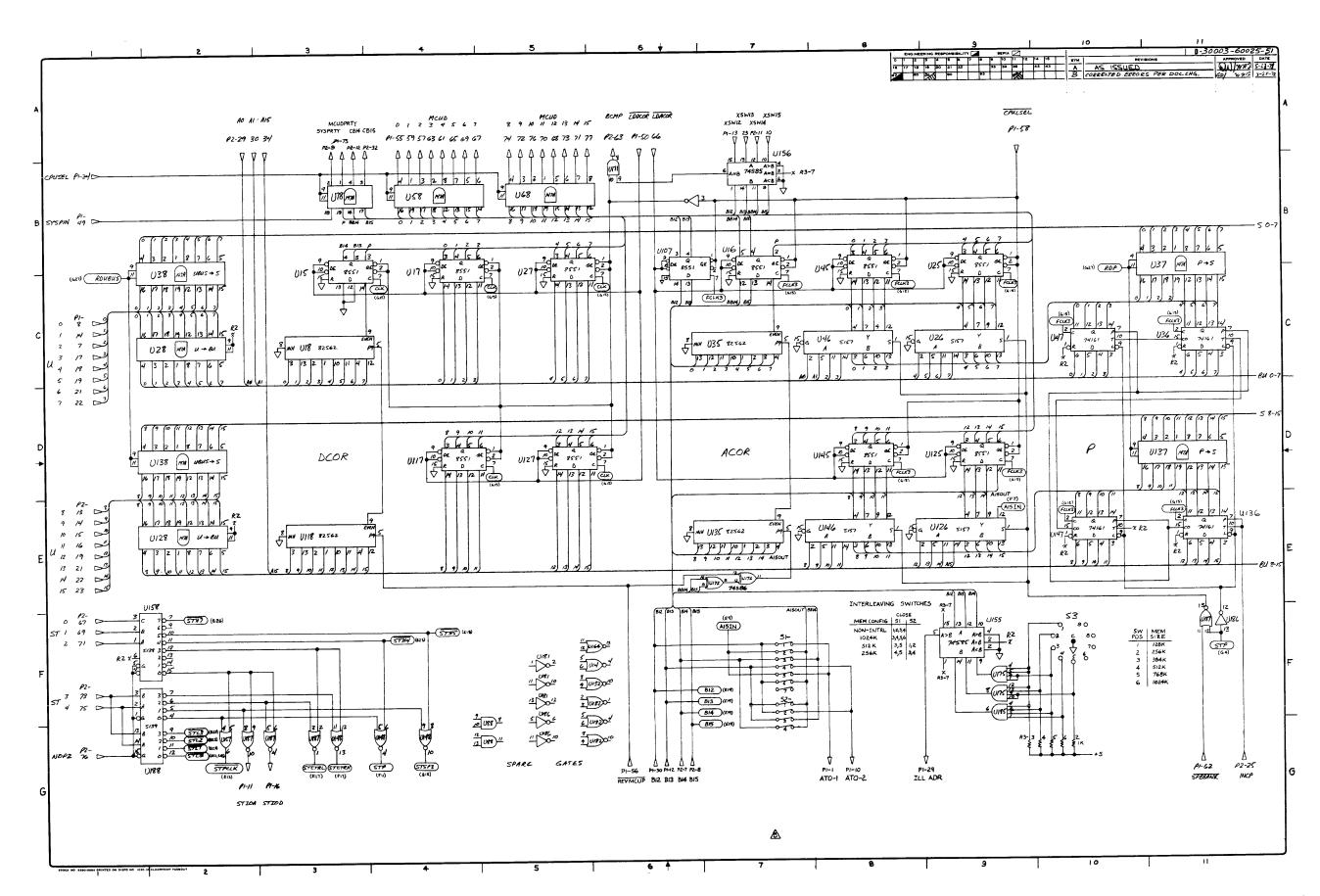


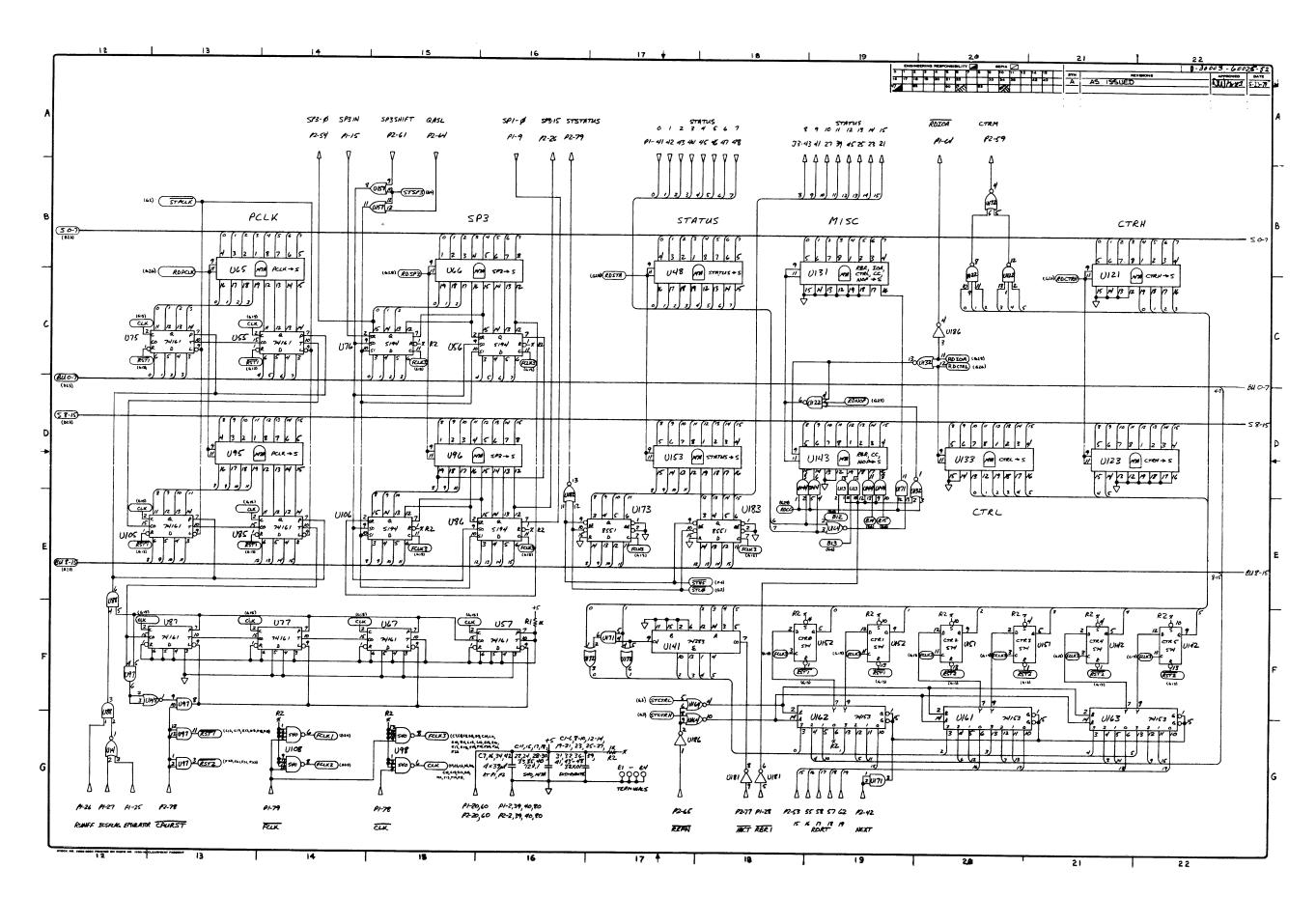


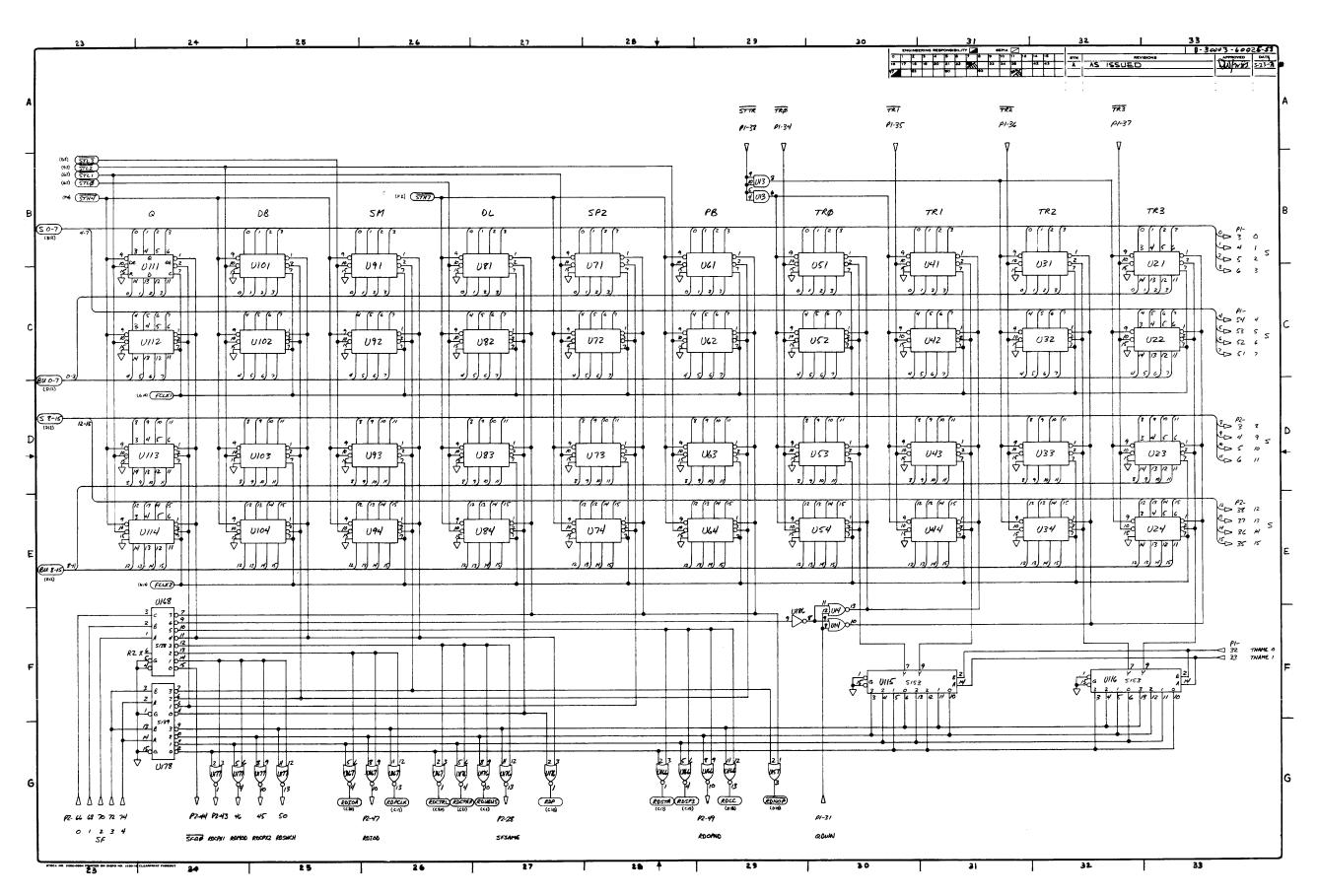


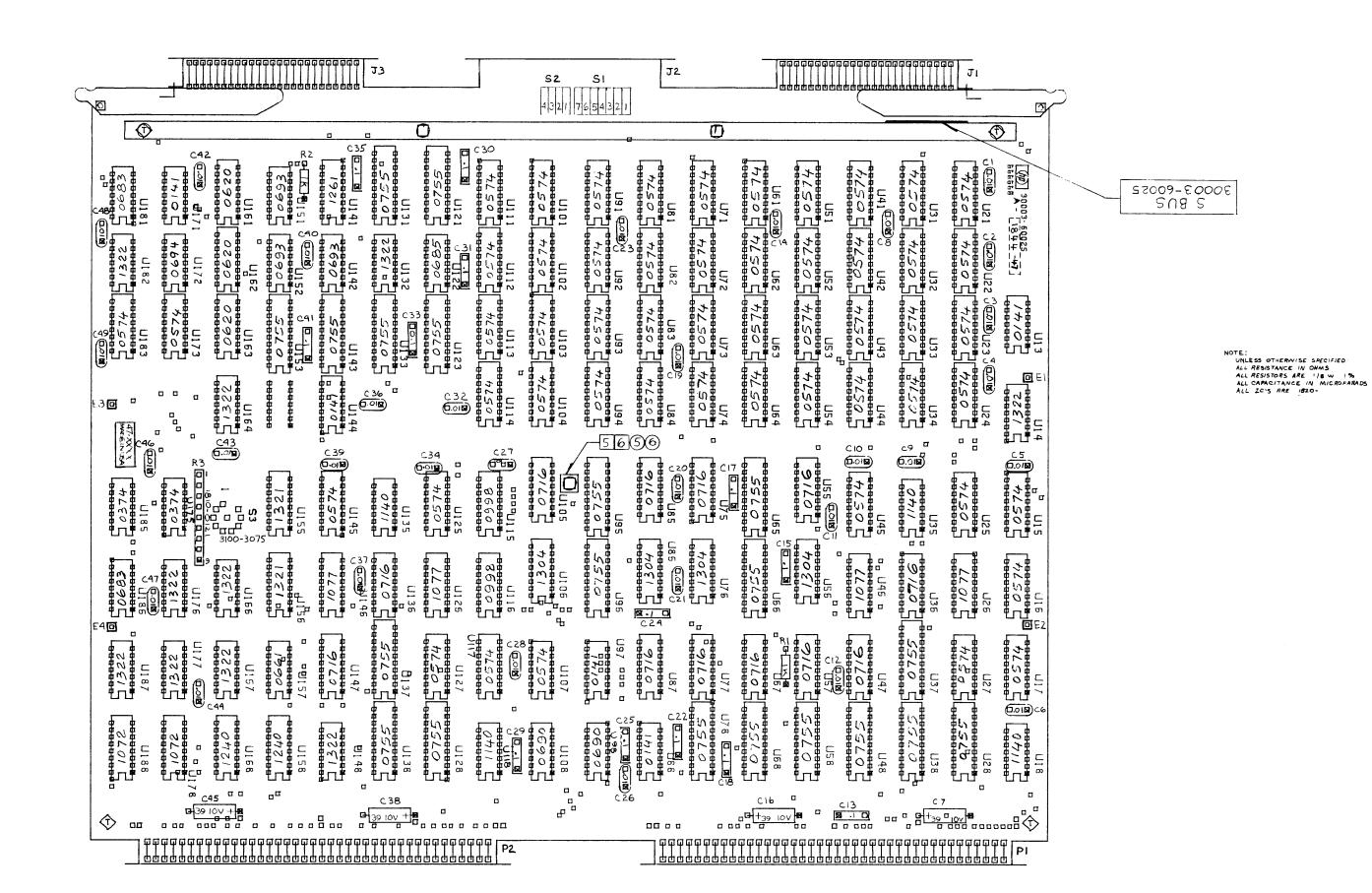


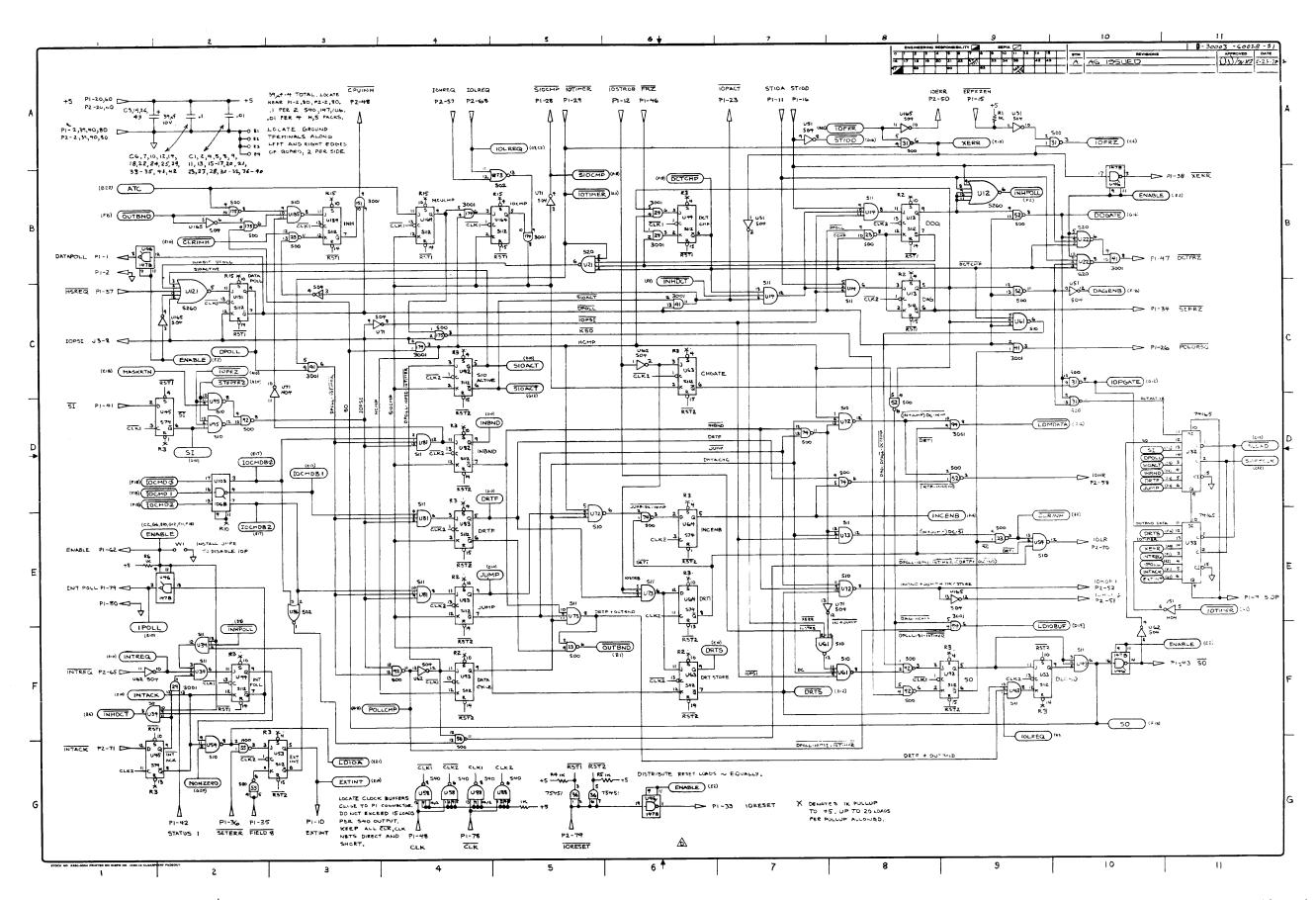


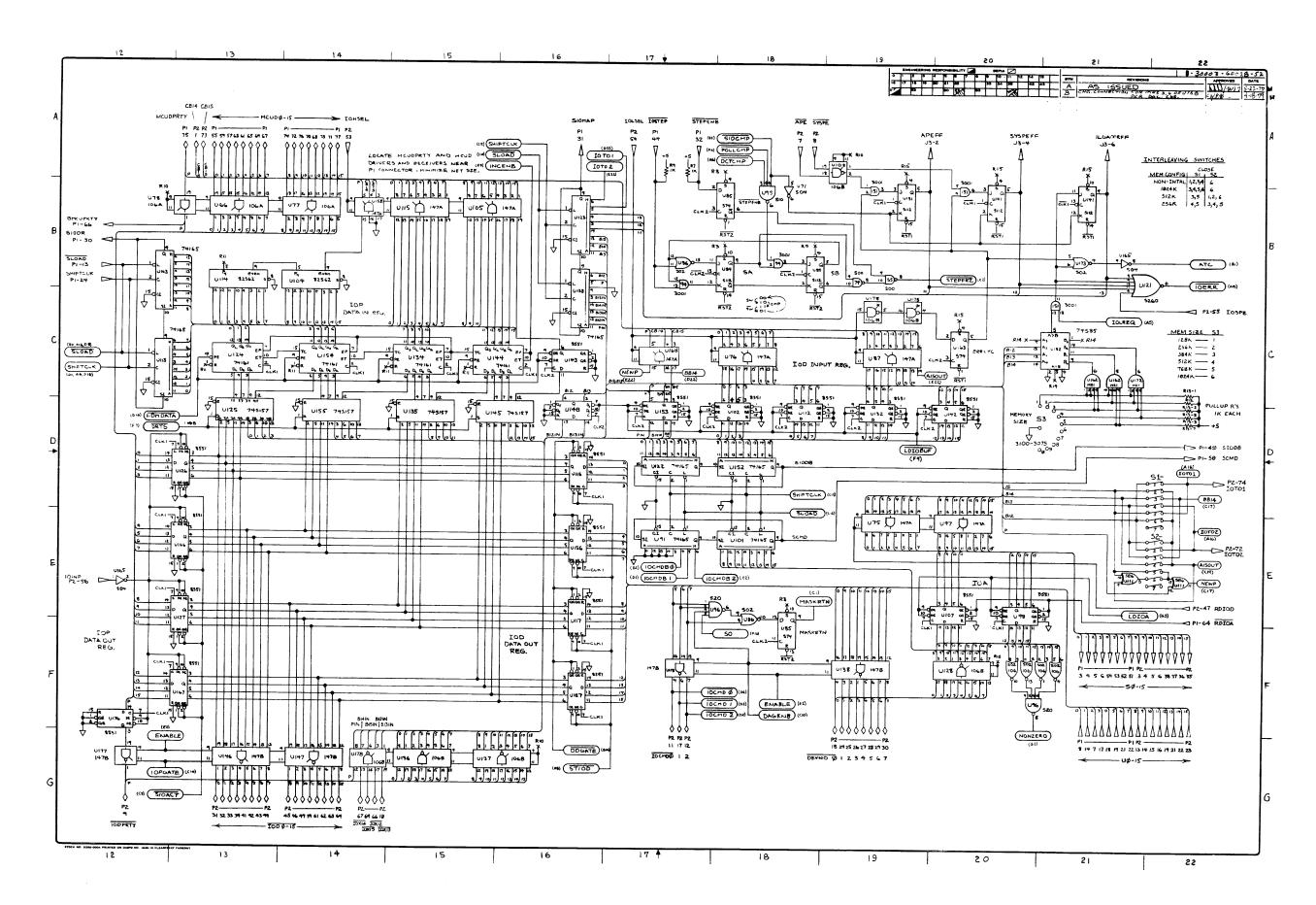


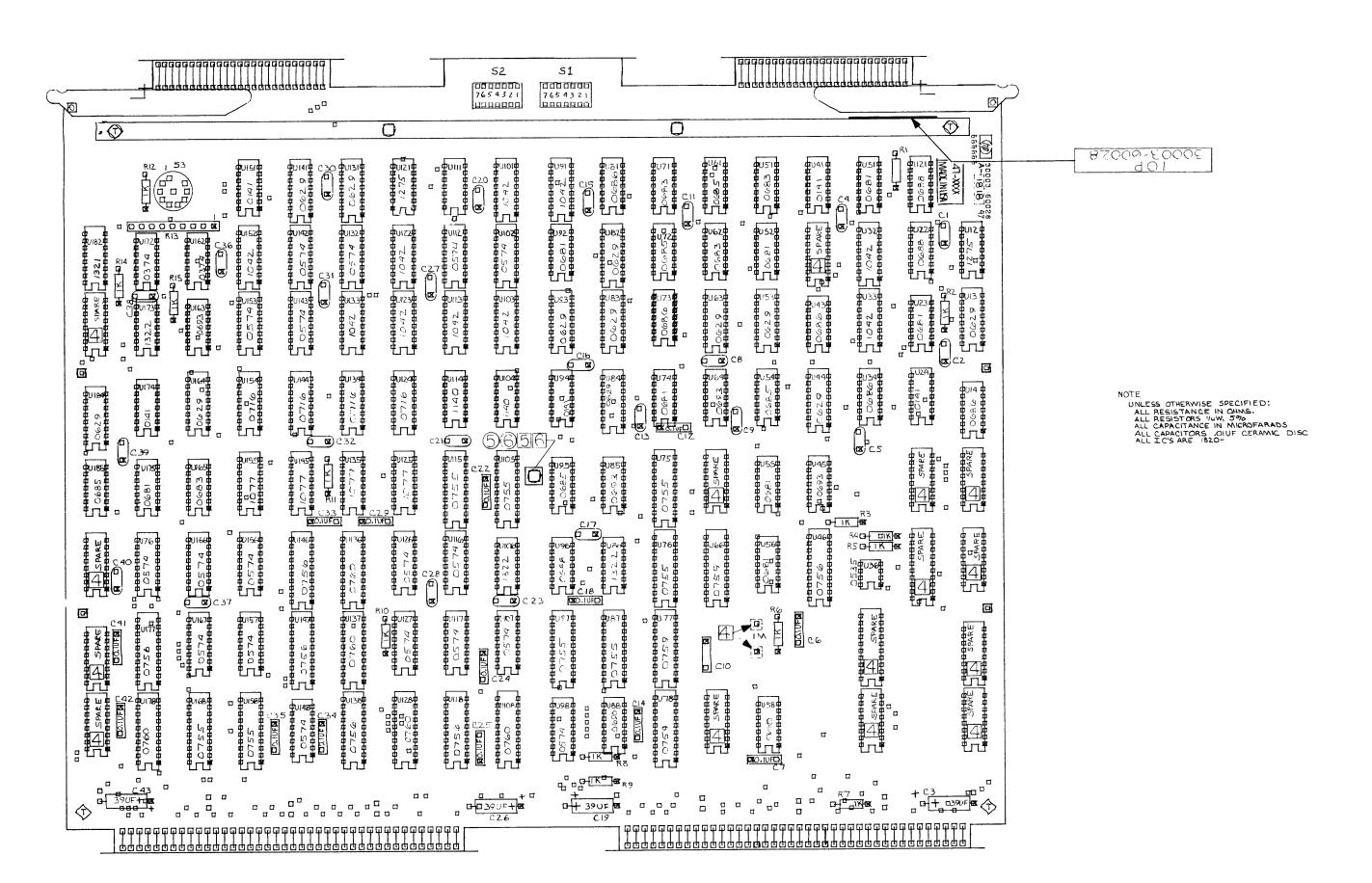


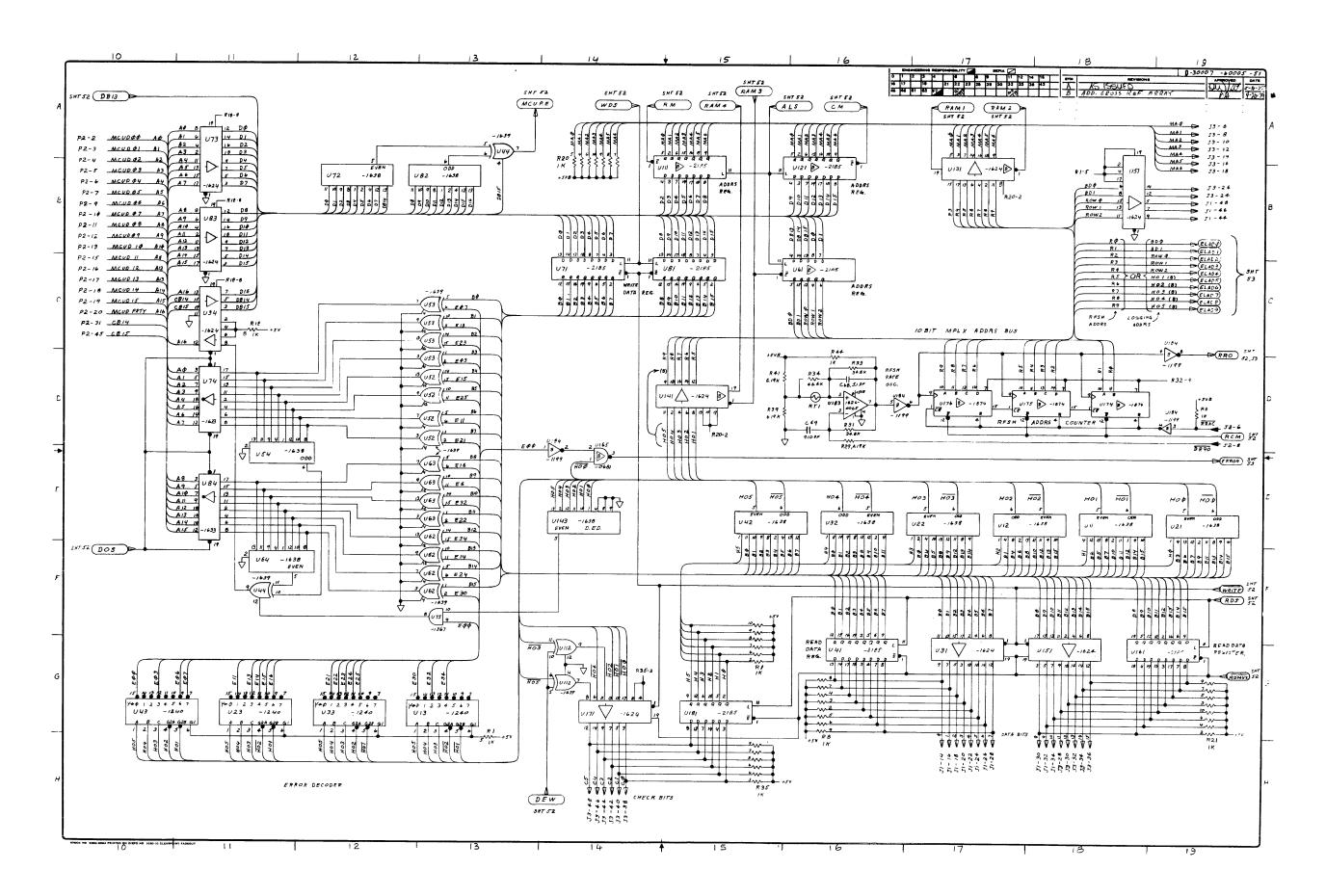


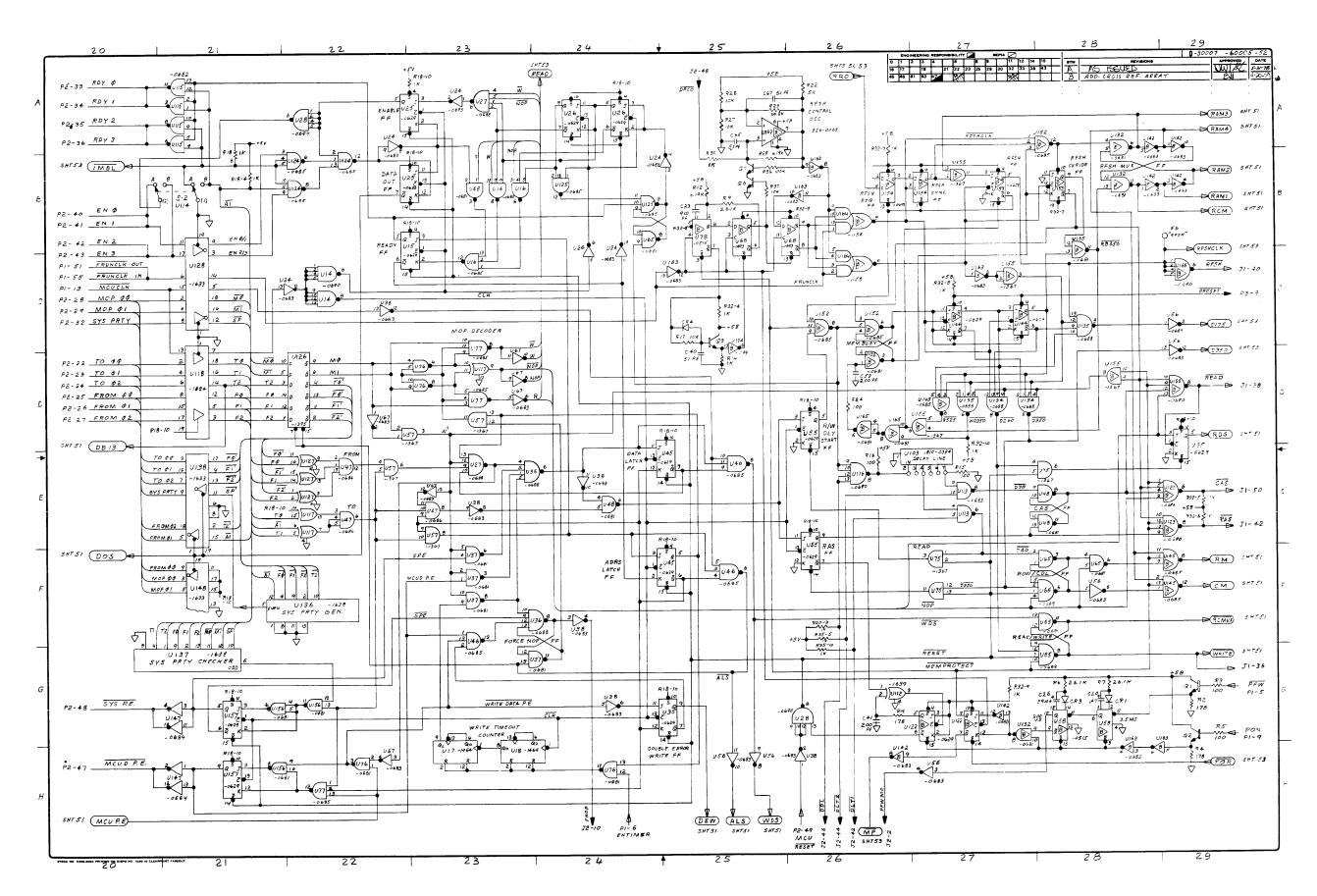


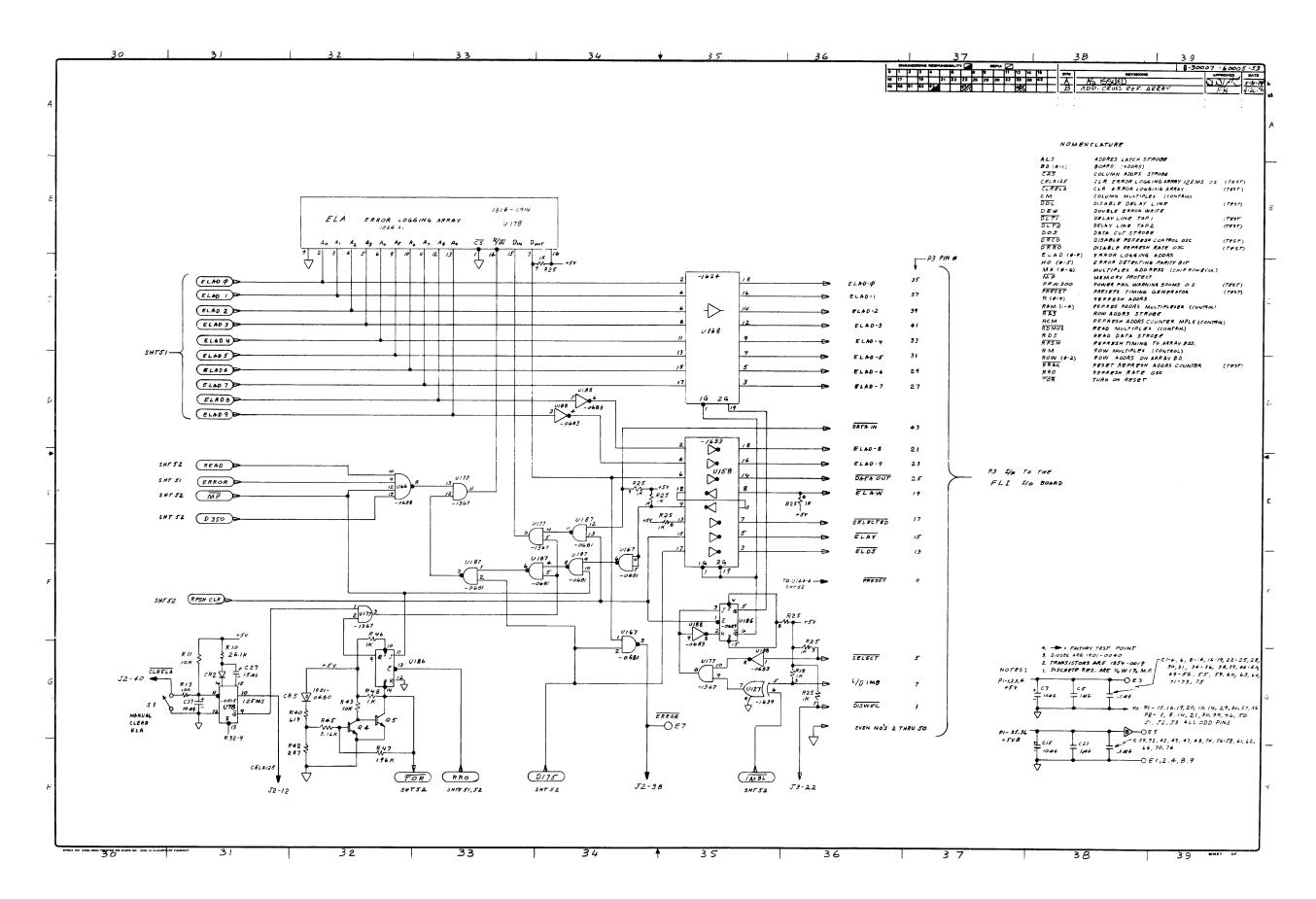


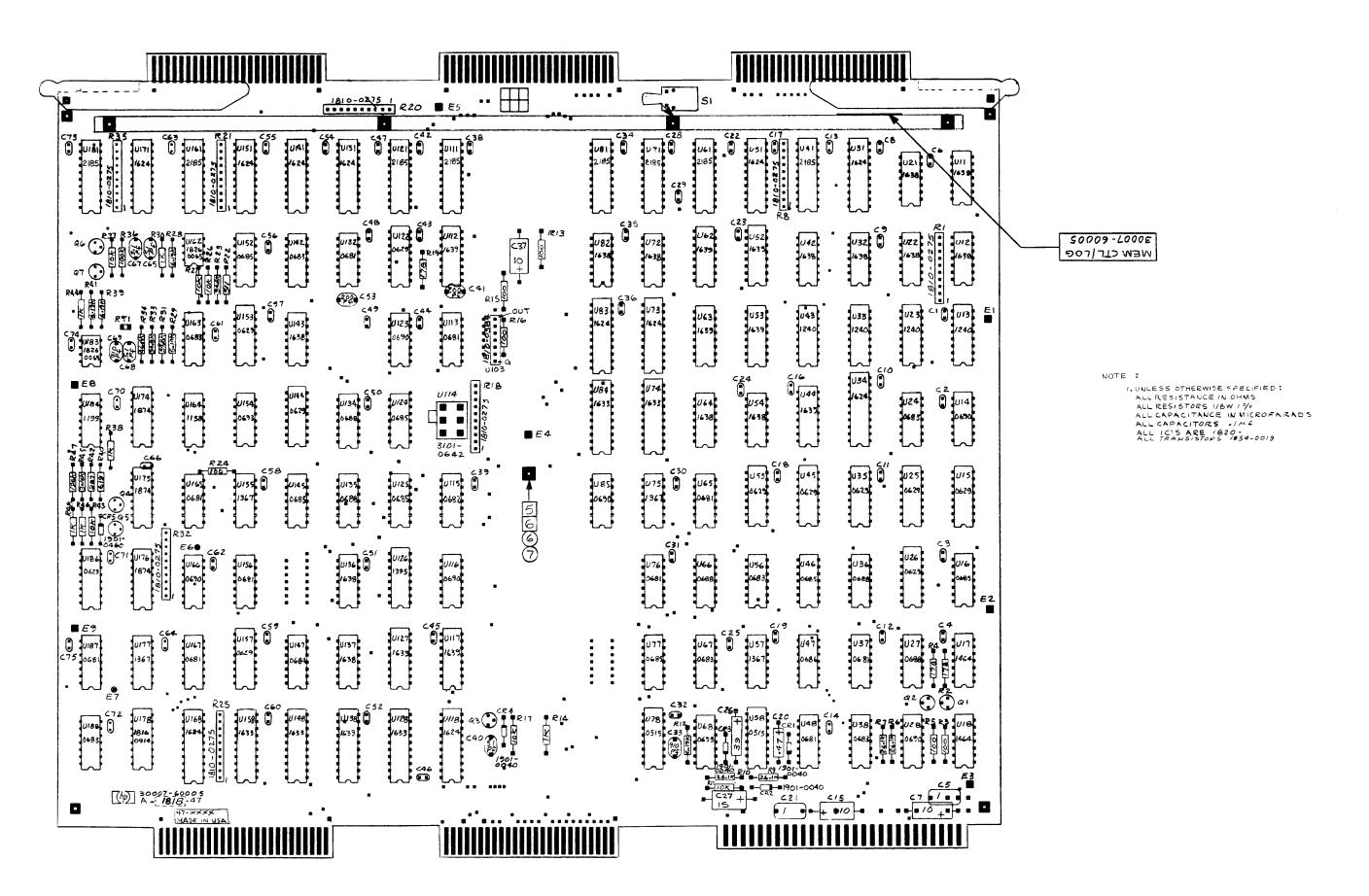


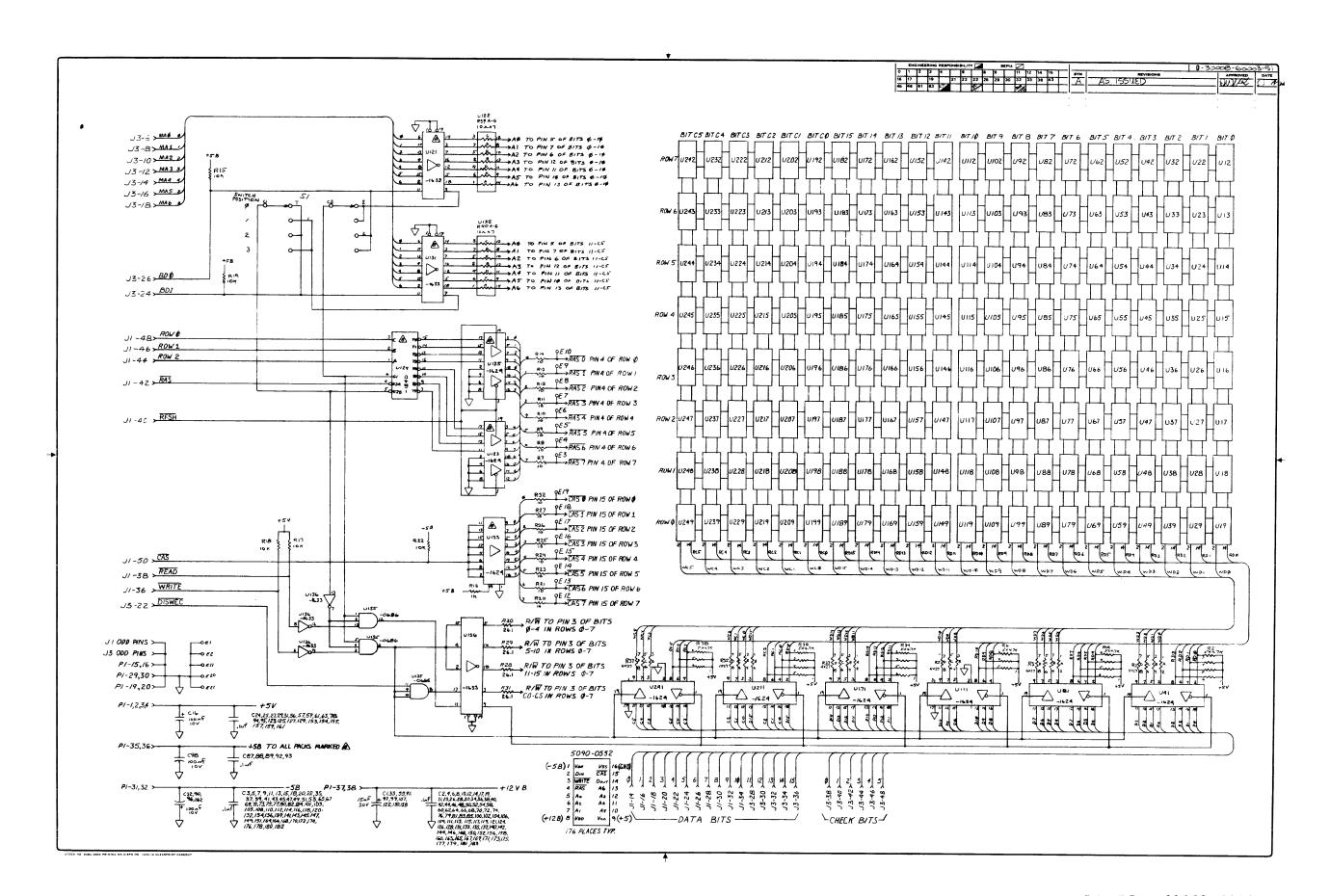


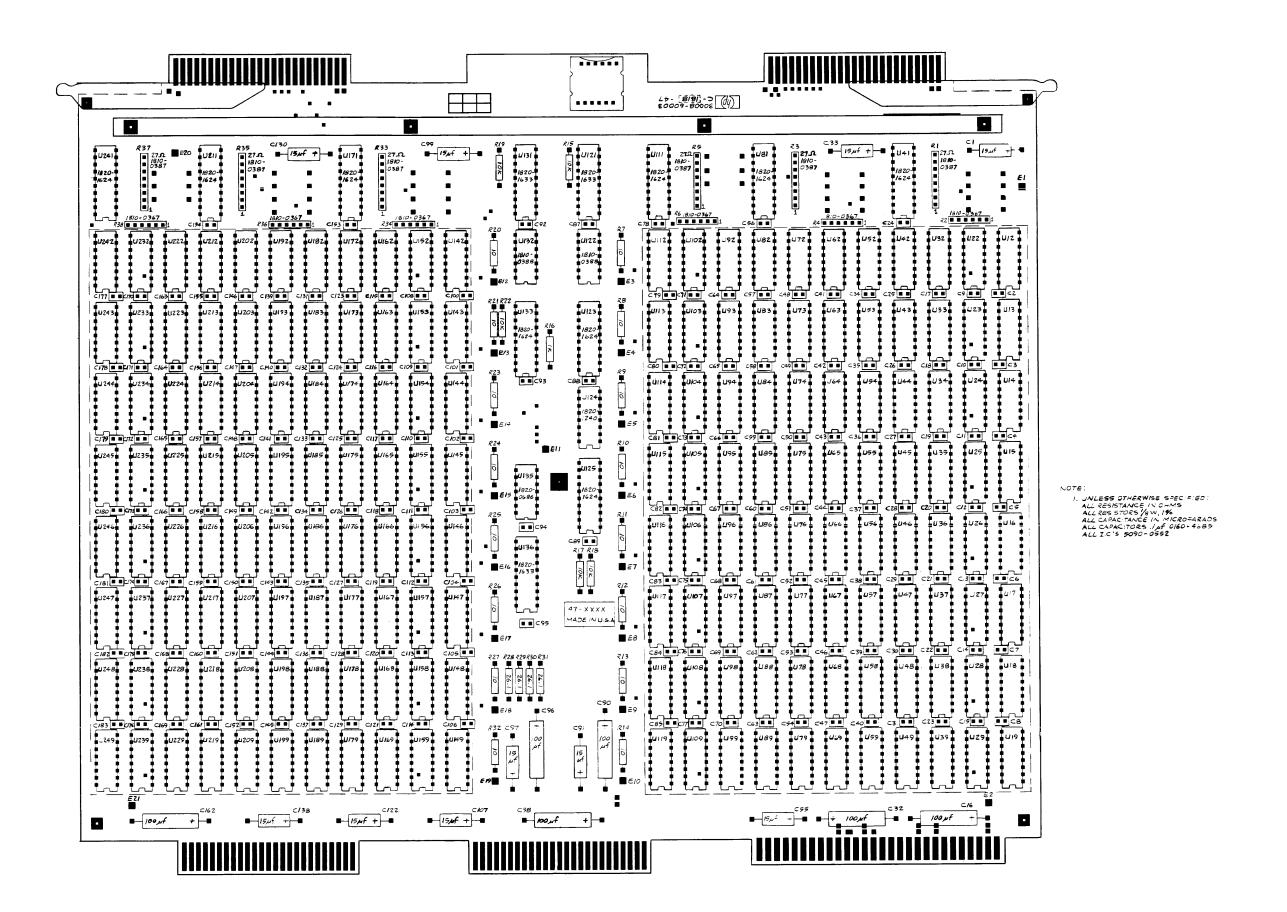


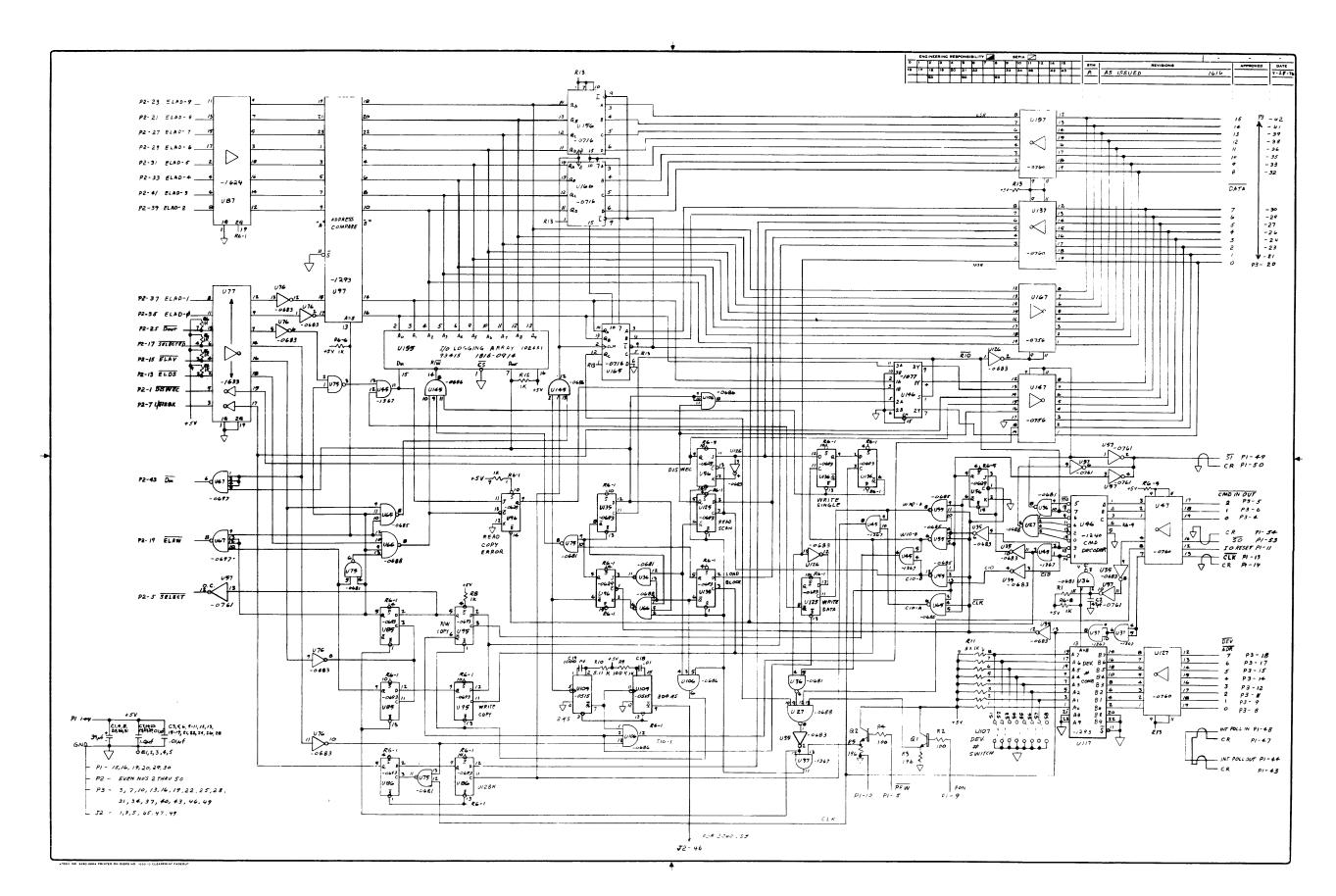


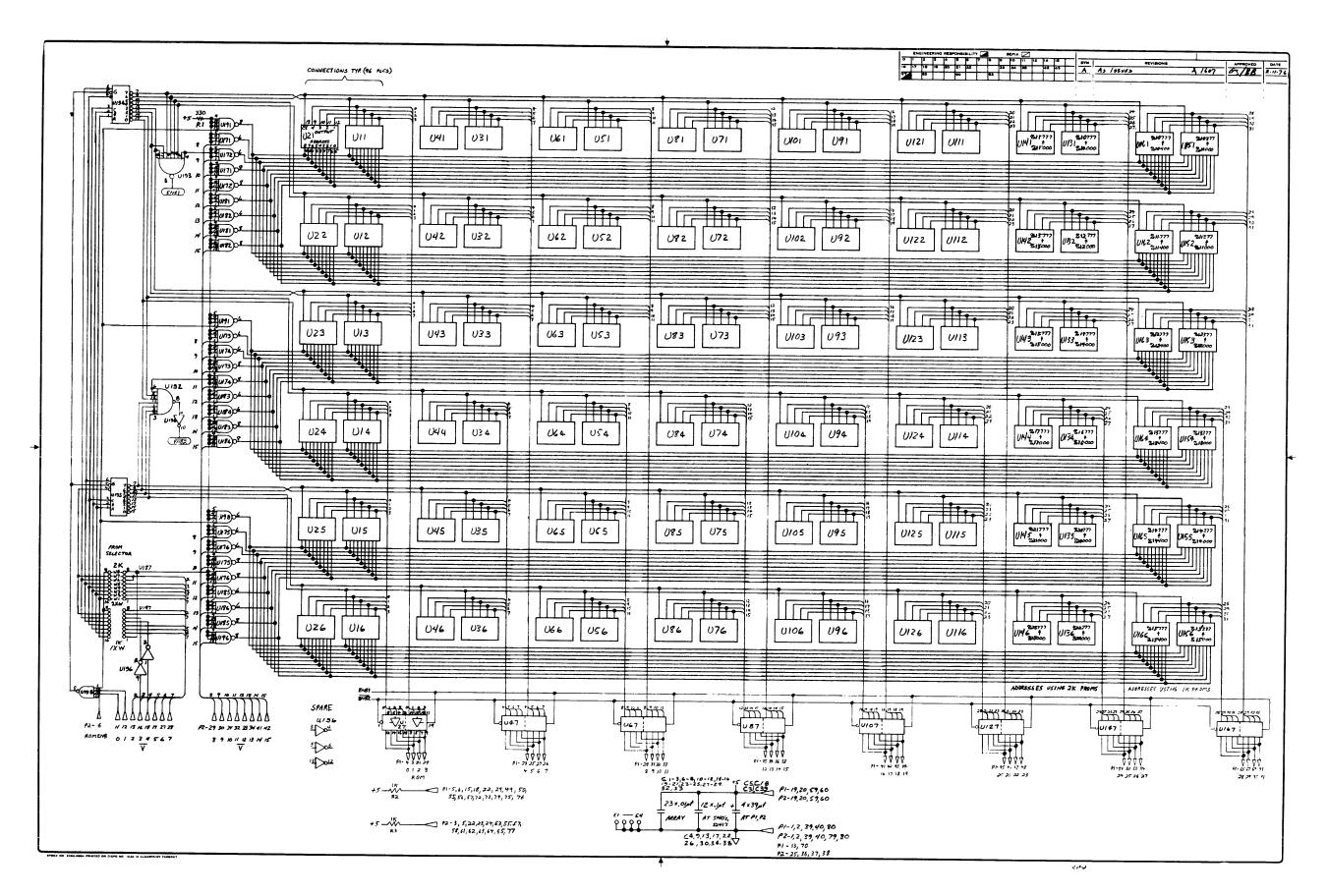


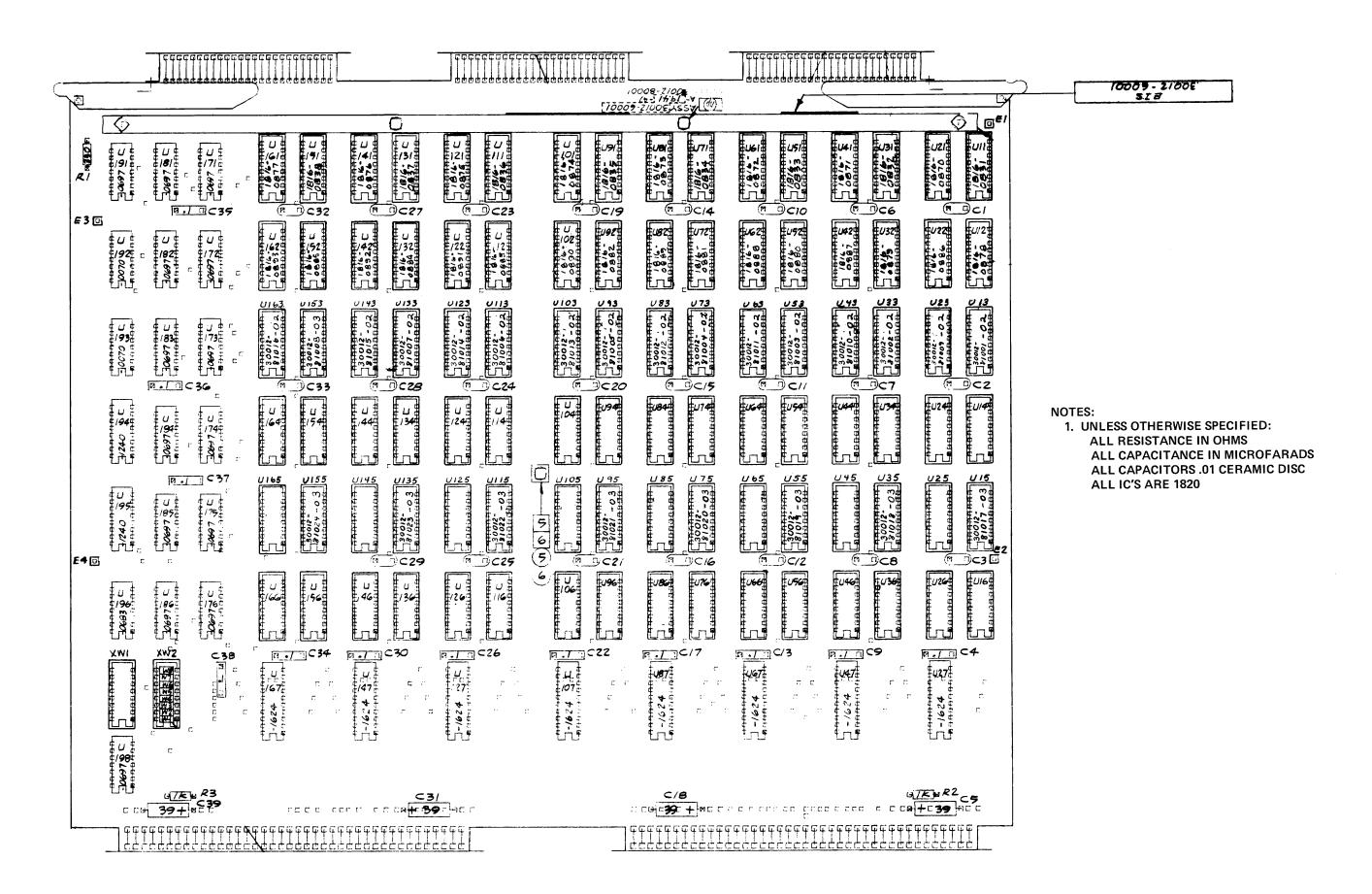








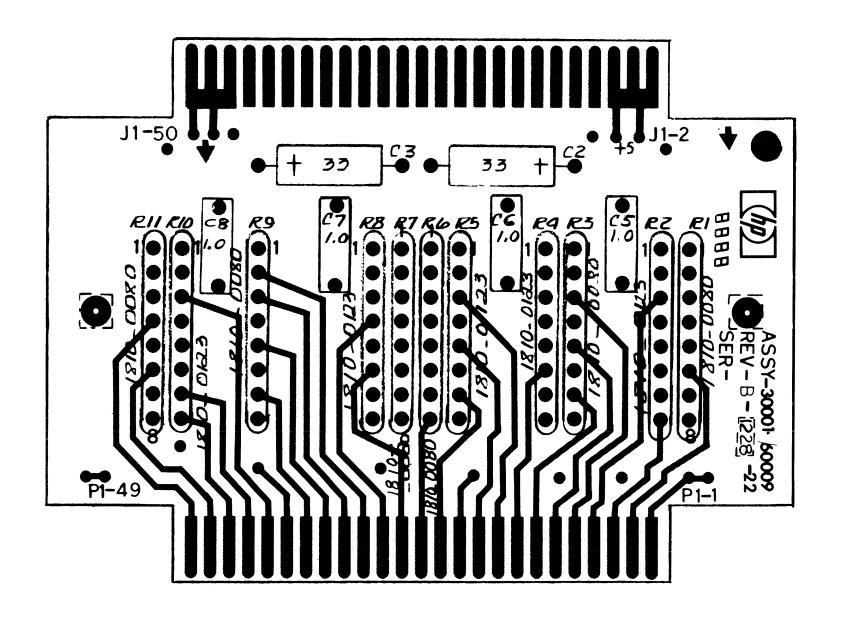




SECTION III - I/O PCAS

CONTENTS

PCA NO.	NAME
30001-60009	ator ator anel —MPU —DCI trol ncer ator ler ster lock facel ance ance mbly fface fface fface Fite Bus
30202-60003	face
30215-60002	ller face face ator mbly face

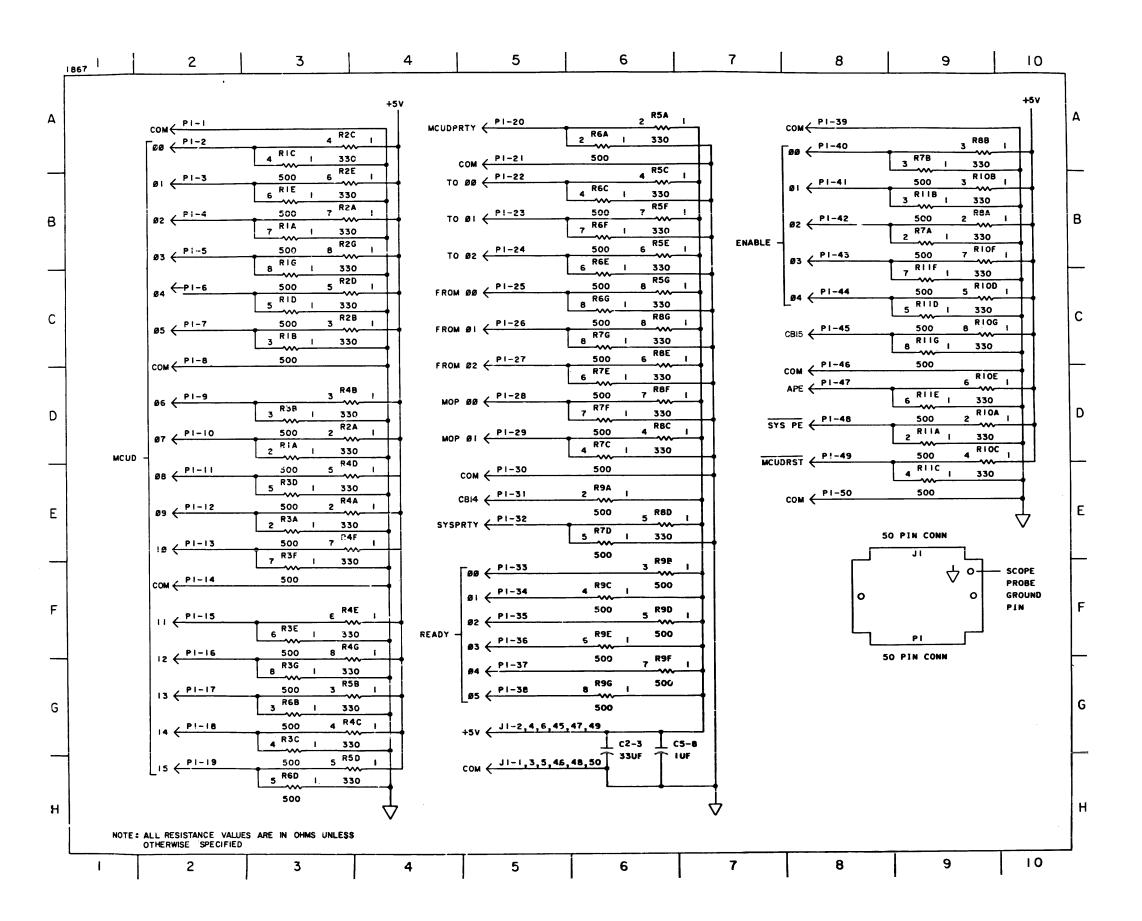


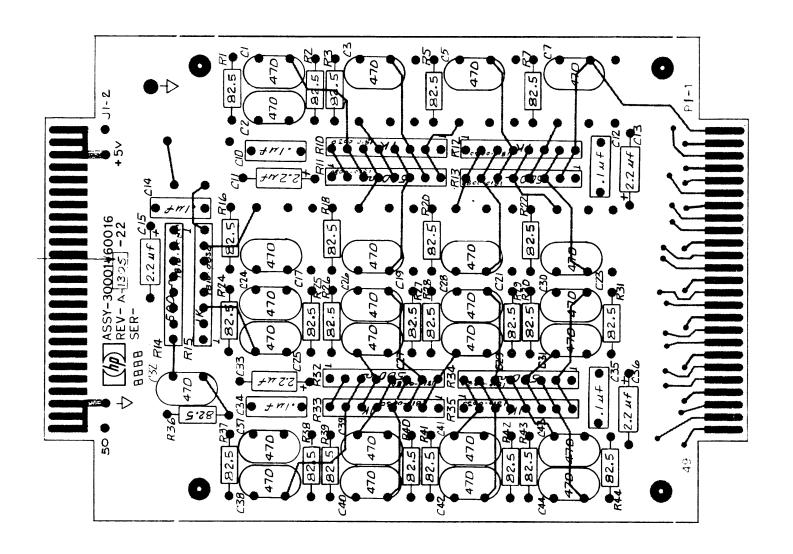
NOTE

UNLESS OTHERWISE SPECIFIED.

ALL CAPACITANCE IN MICROFAKAUS.

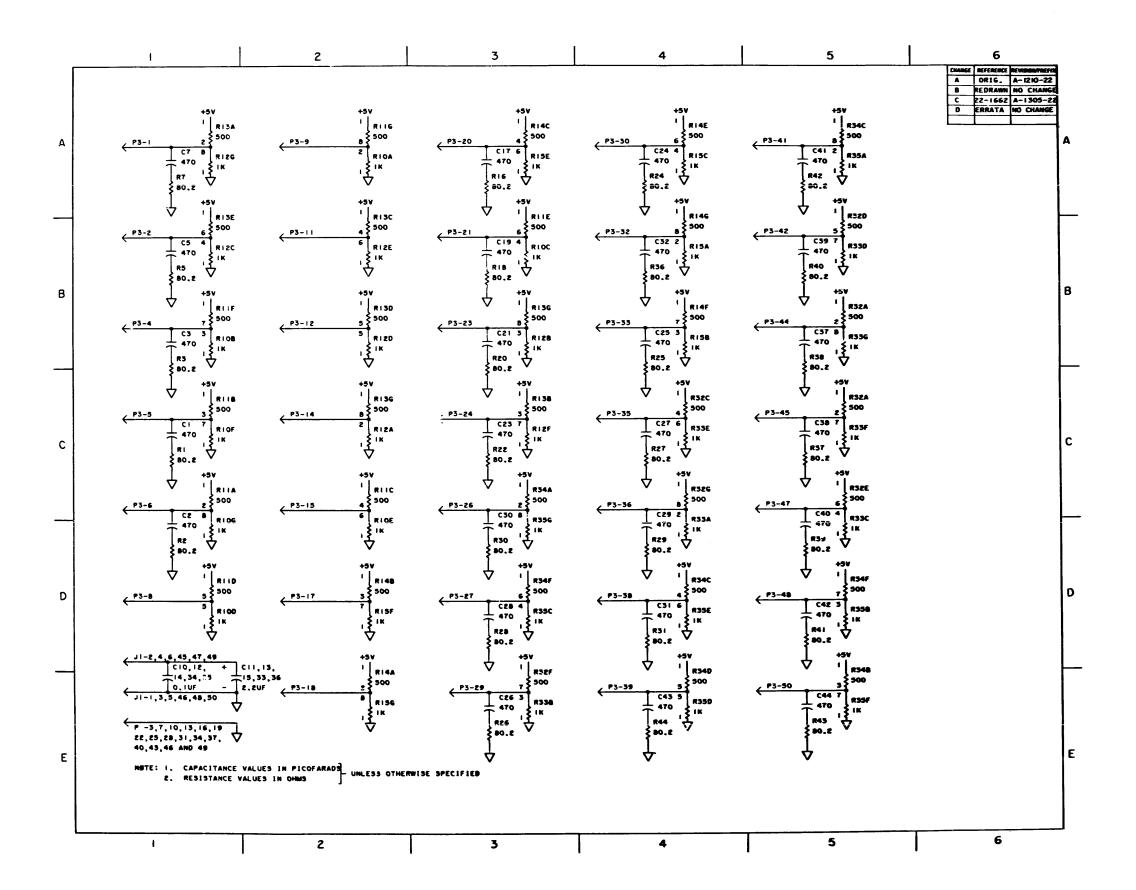
ALL RESISTANCE IN SHMS.

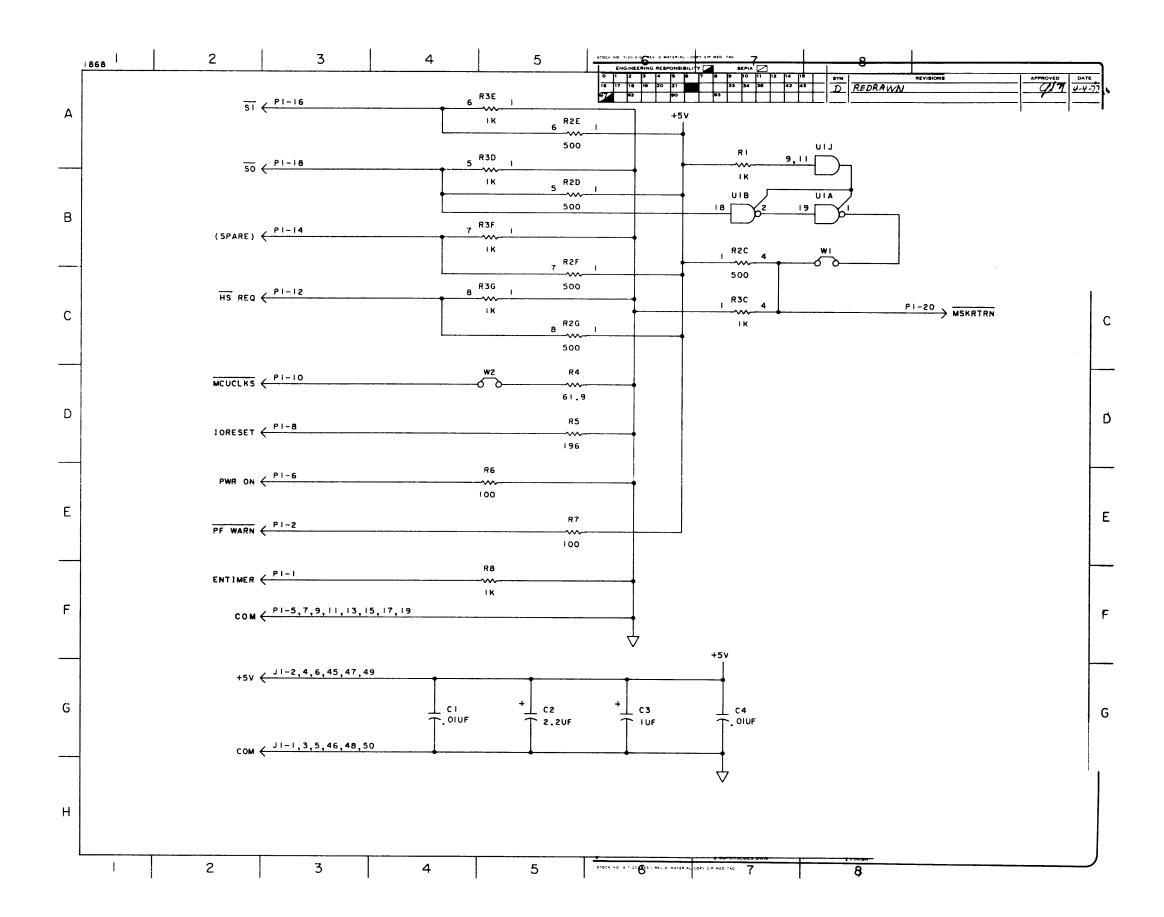


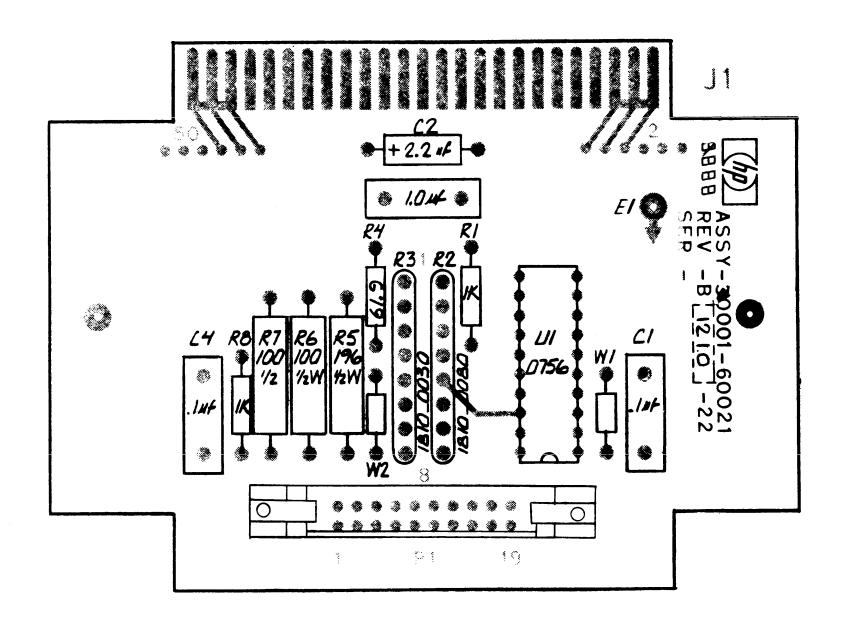


NOTE;

I. UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IN OHMS
ALL RESISTORS YOW 1% M F.
ALL CAPACITANCE IN PICOFARADE

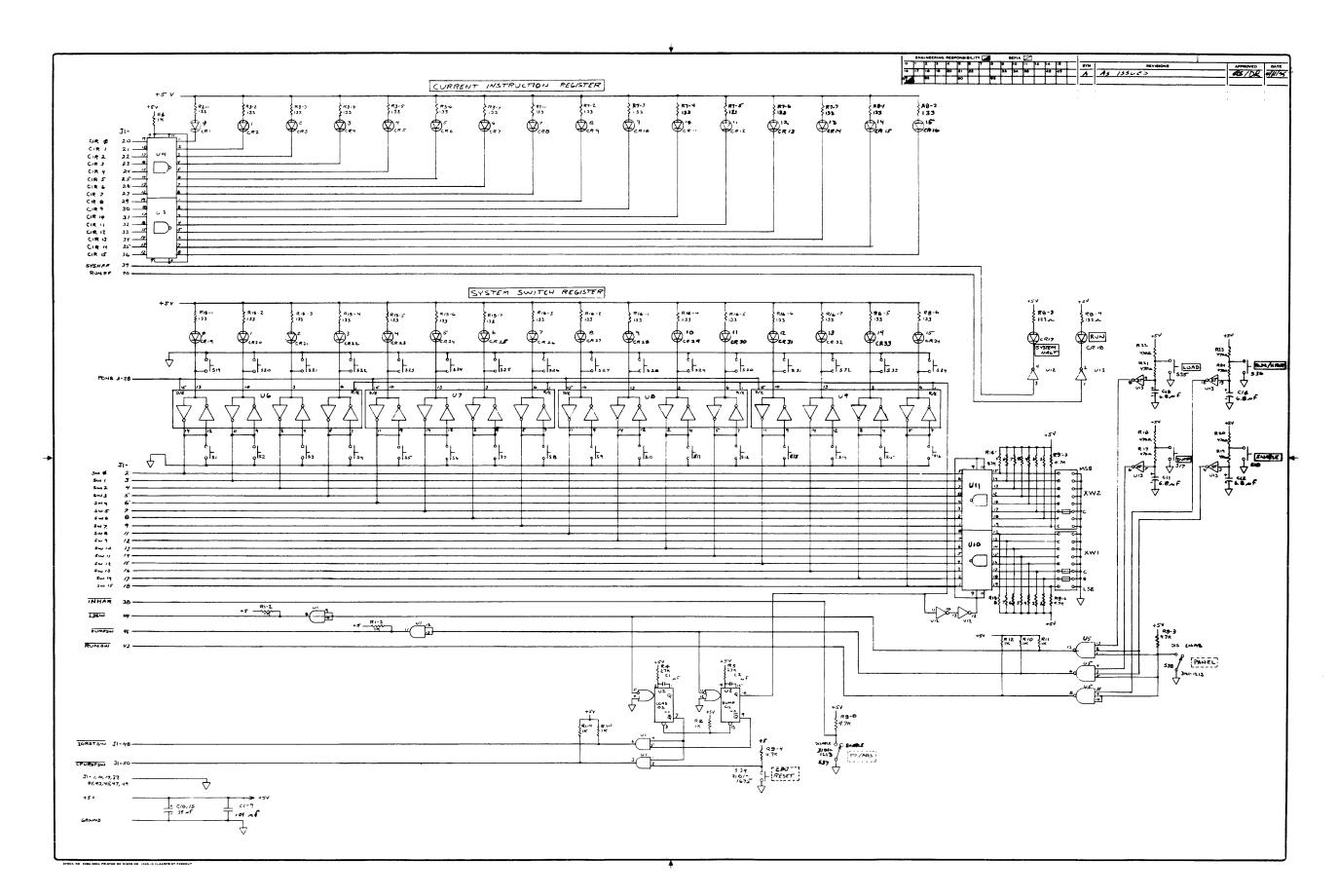


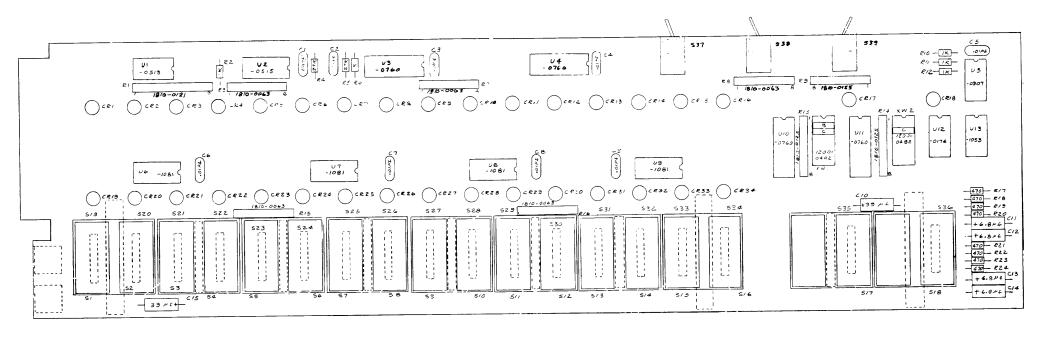




NOTE

UNLESS OTHERWISE SPECIFIED
ALL CESISTANCE IN OHMS
ALL RESISTORS 14W_1%_MF
ALL CAPACITANCE IN MICEO_FACADS





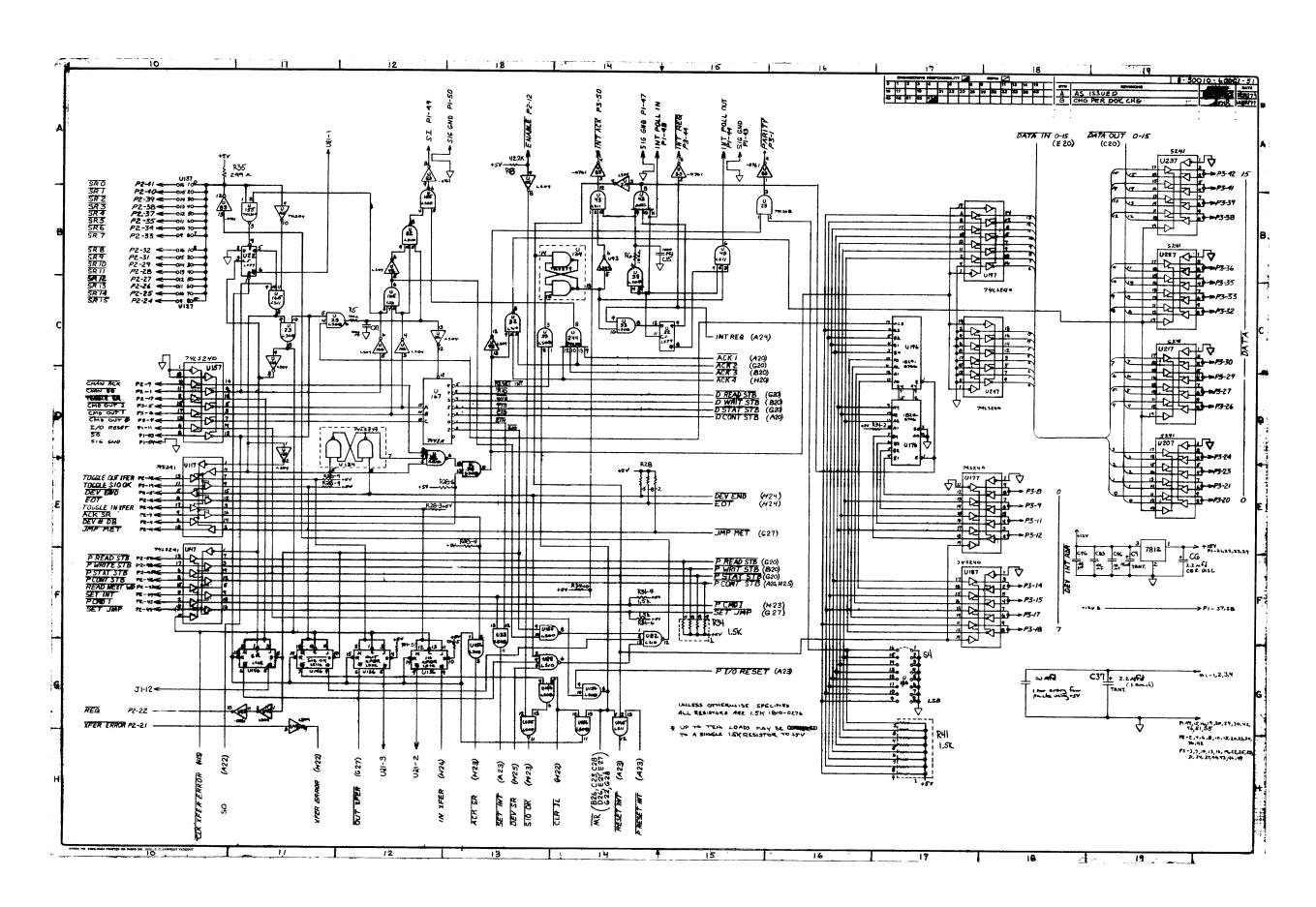
NOTES :

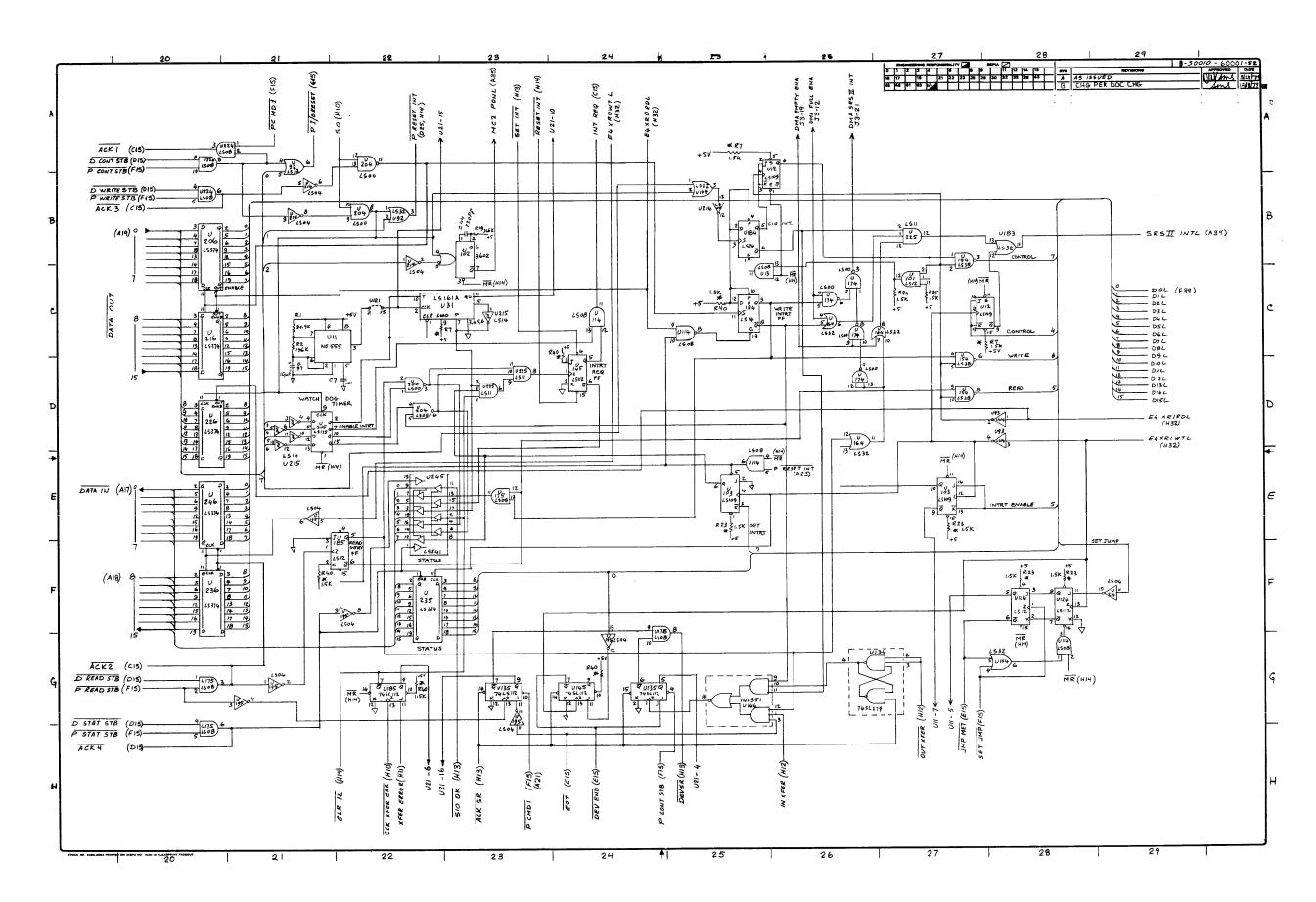
I. UNLESS OTHERWISE SPECIFIED ;

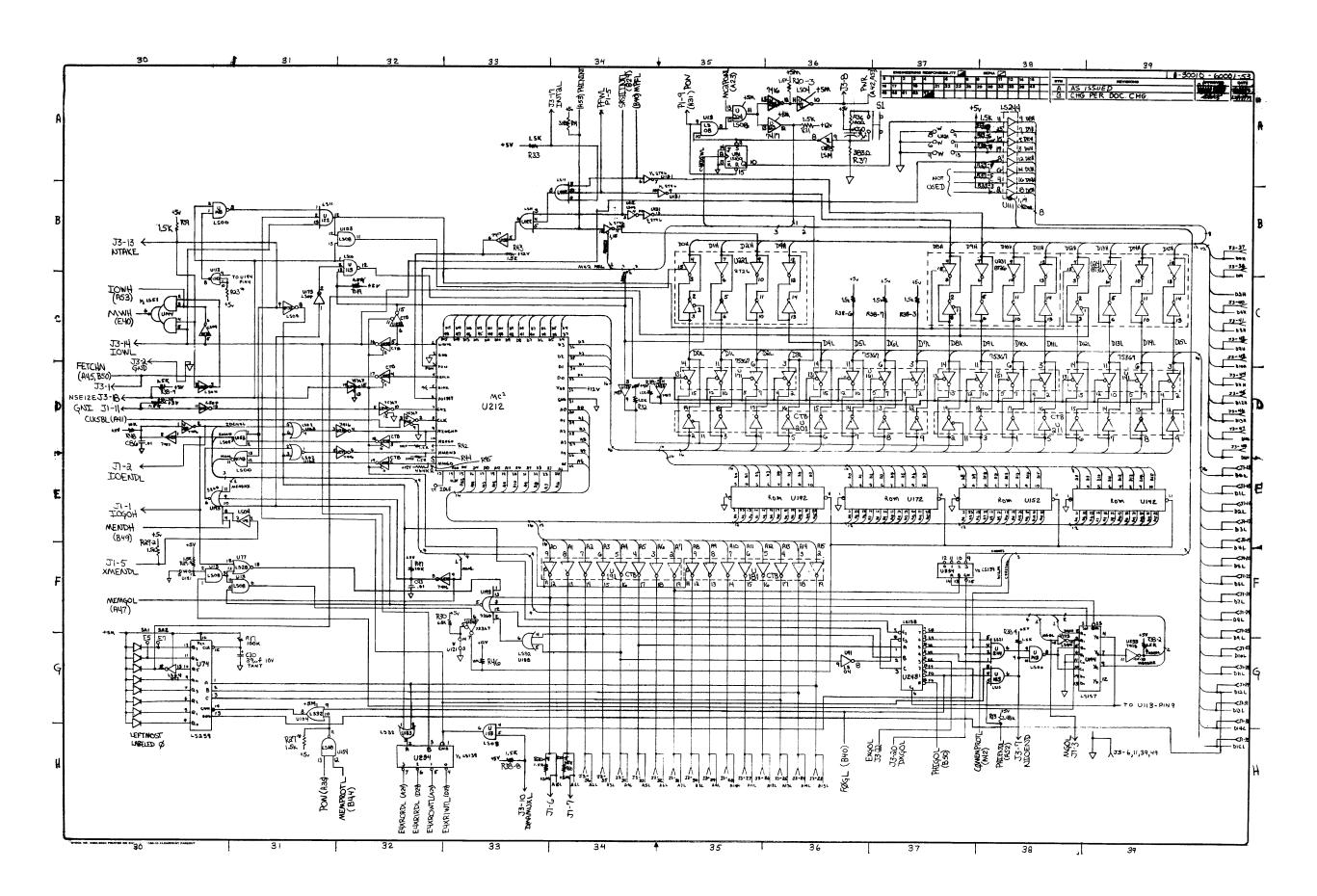
ALL RESISTANCE IV OMMS

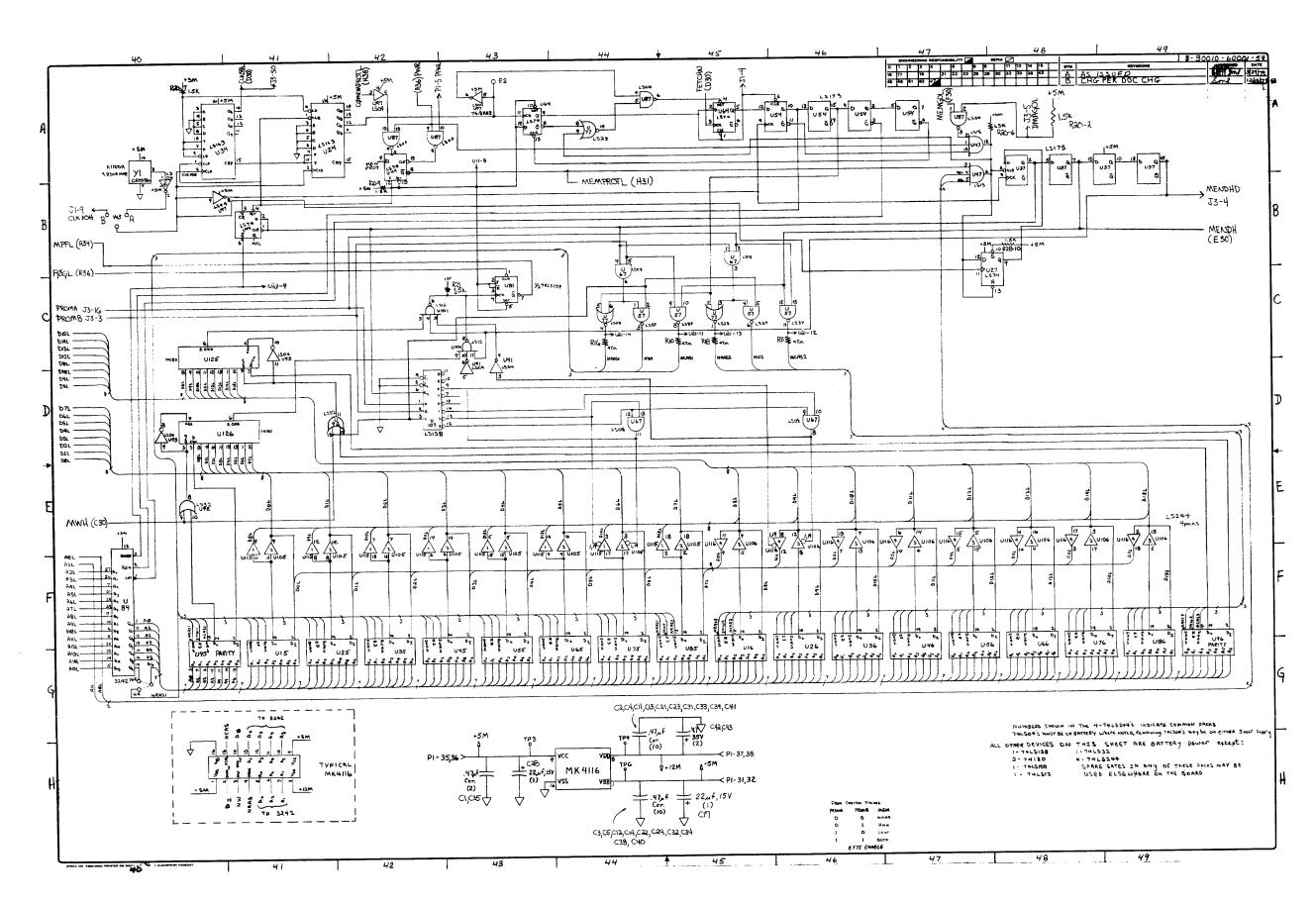
ALL PESISTORS 1/4W, 5 1/4

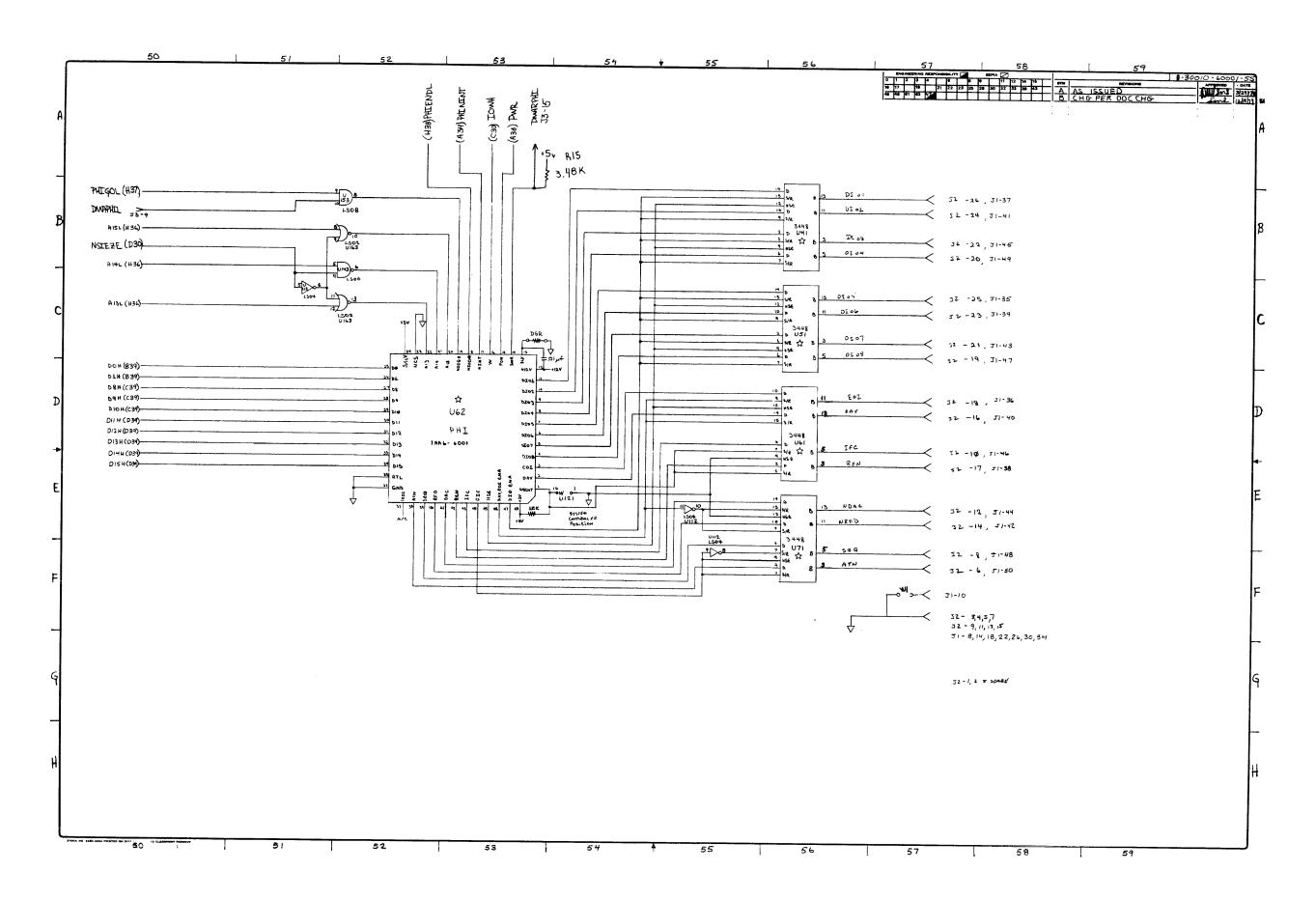
ALL DIODES 1990-0325

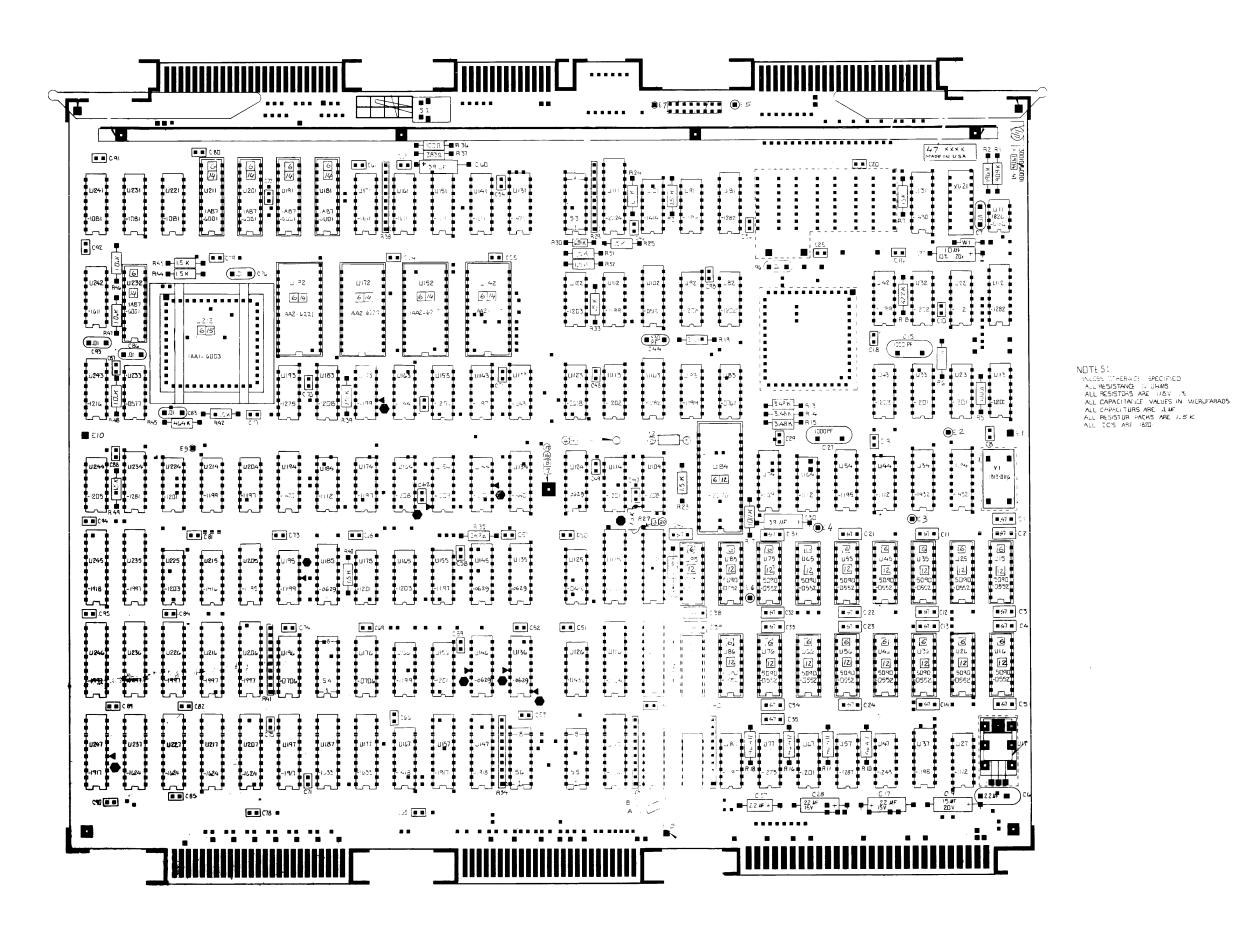


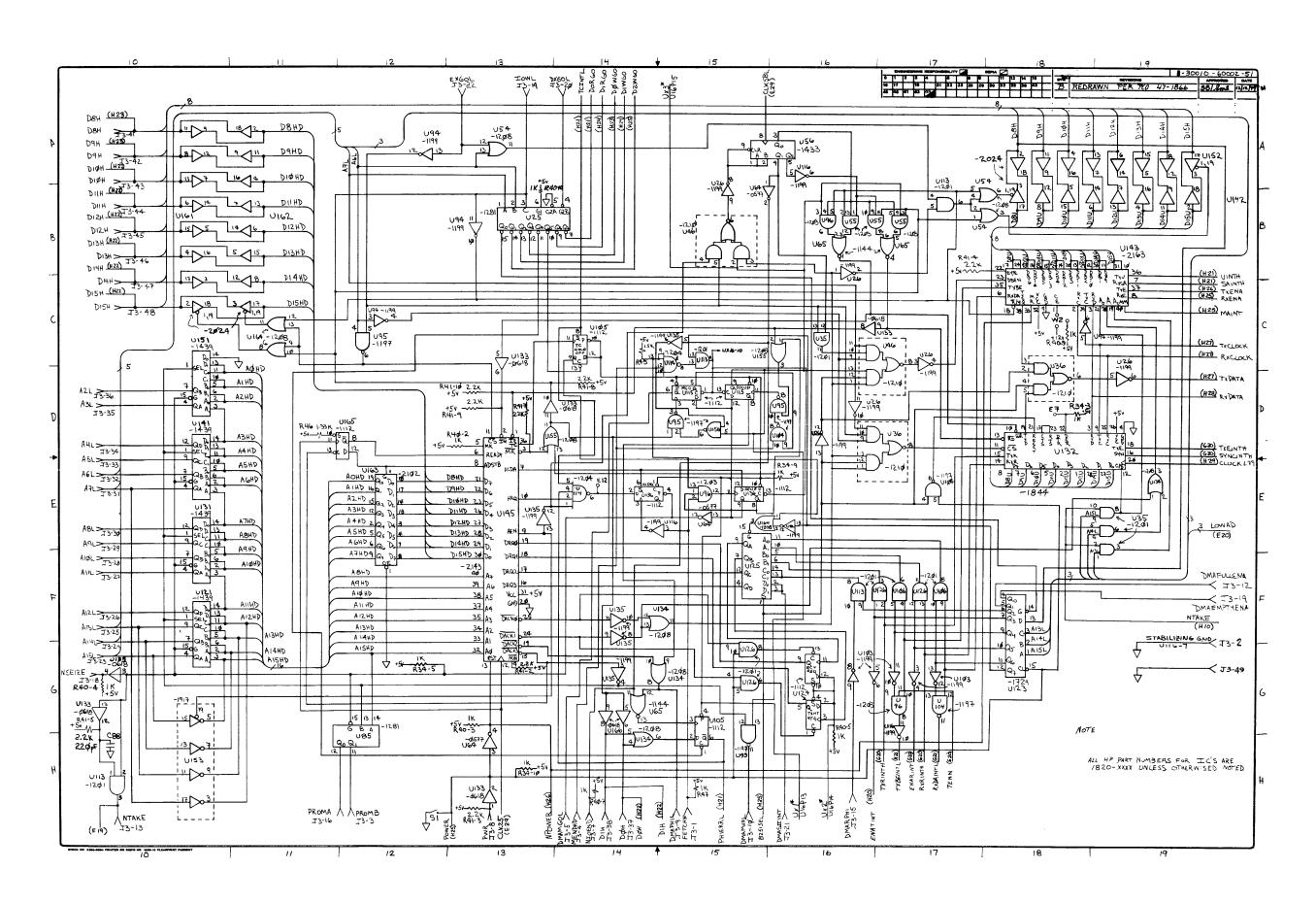


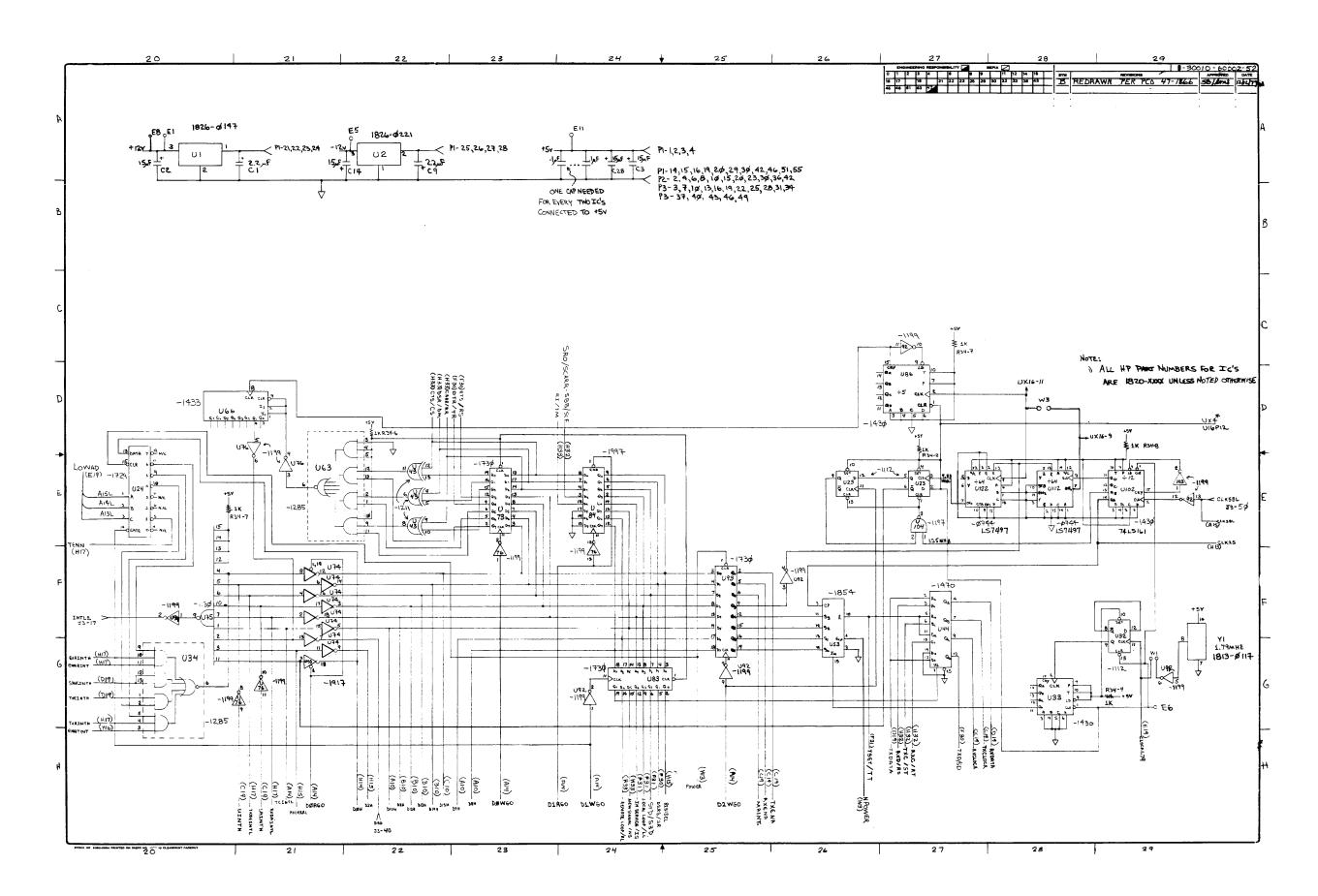


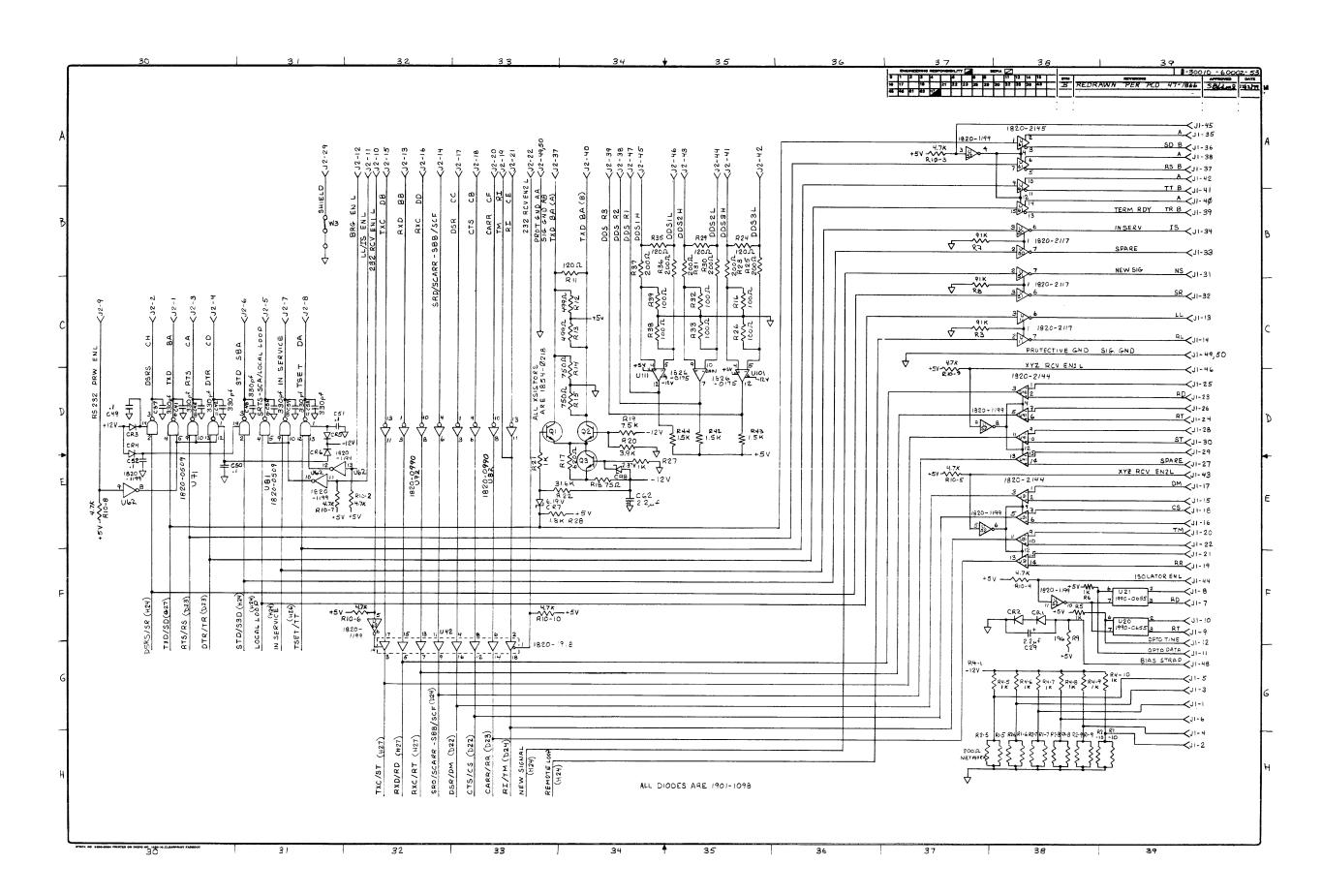


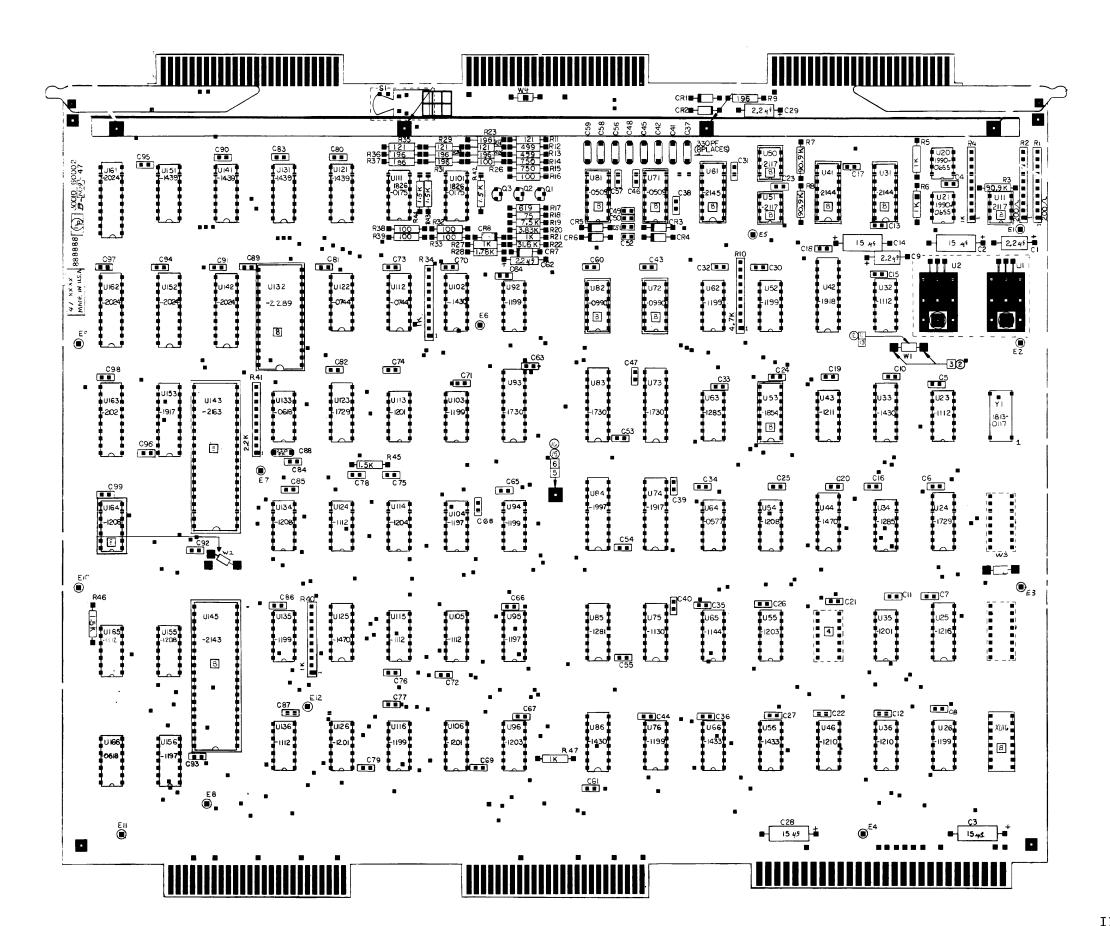




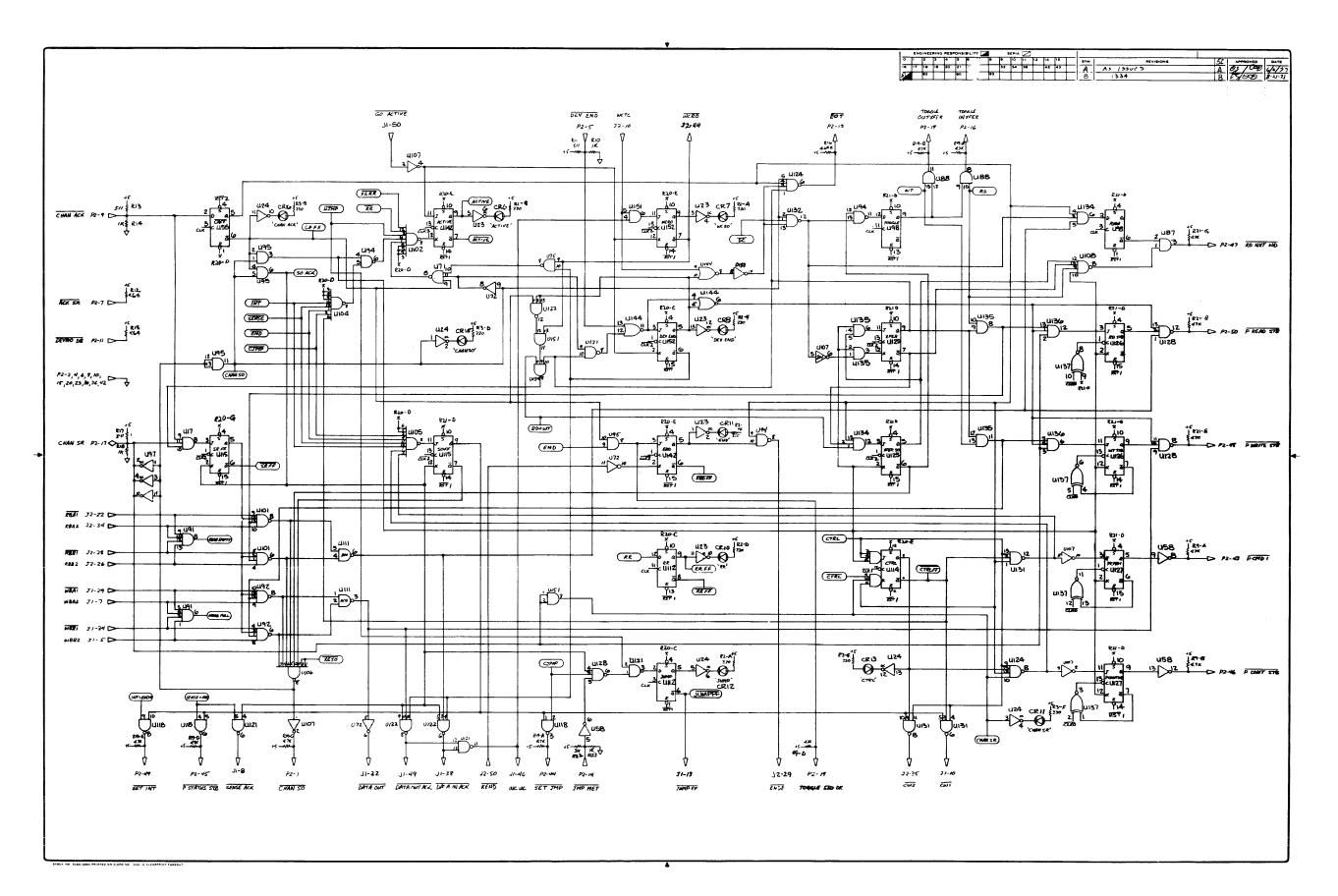


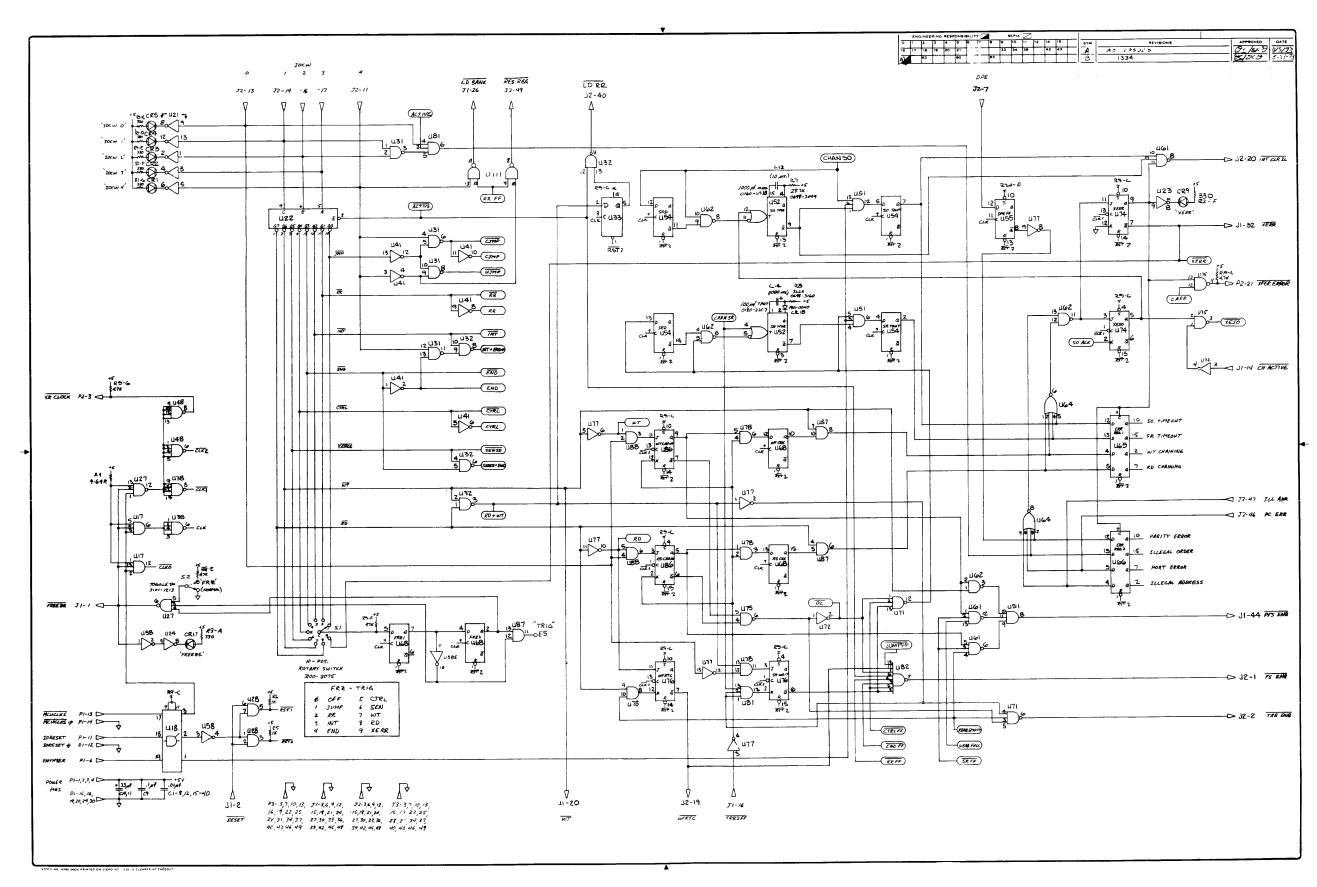




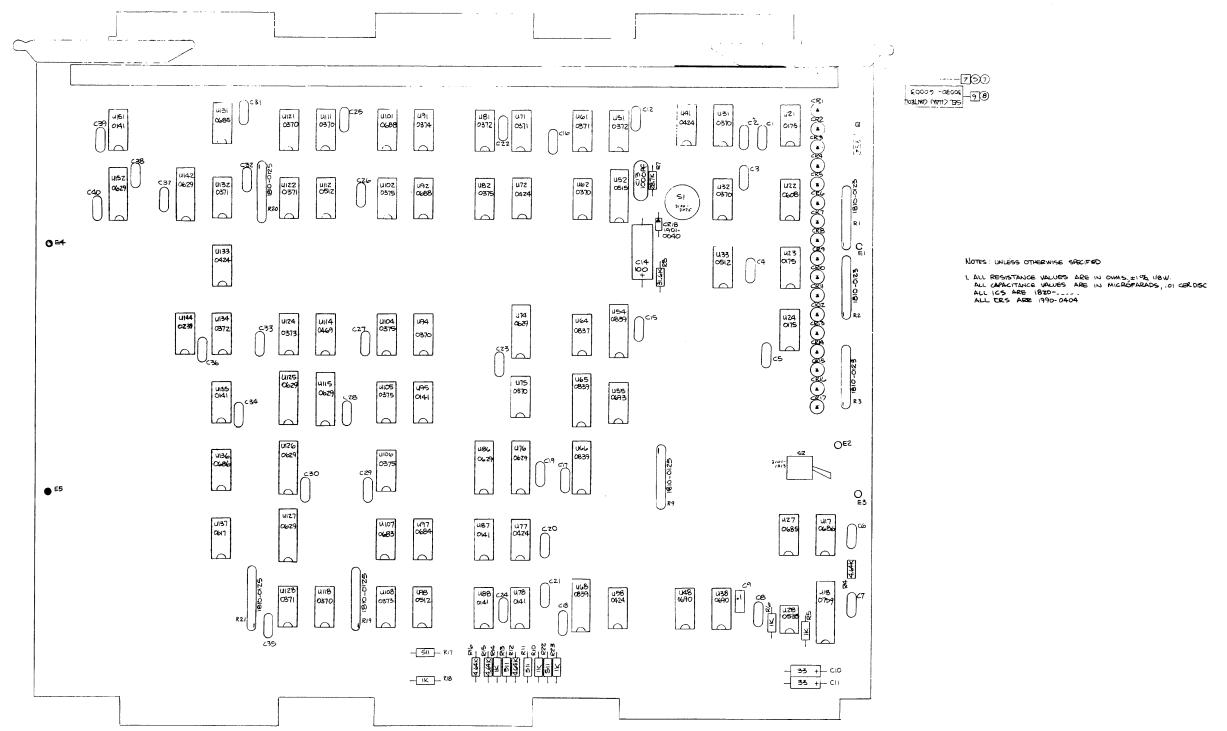


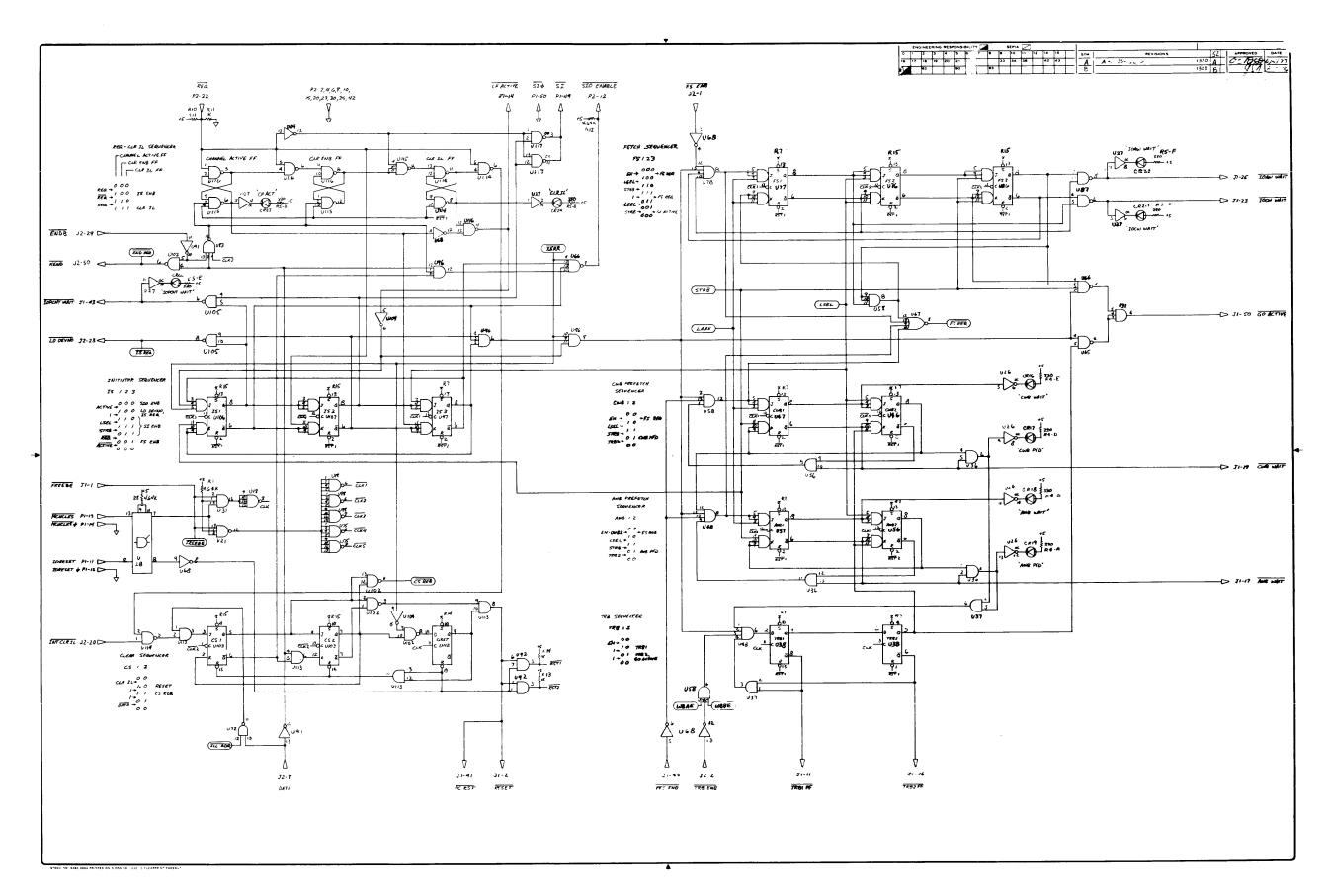
- UNLESS OTHERWISE SPECIFIED: ALL RESISTANCE IN OHMS ALL RESISTORS 1/8 W, 196 ALL CAPACITORS ARE ... UF
- ALL IC'S ARE 1820-

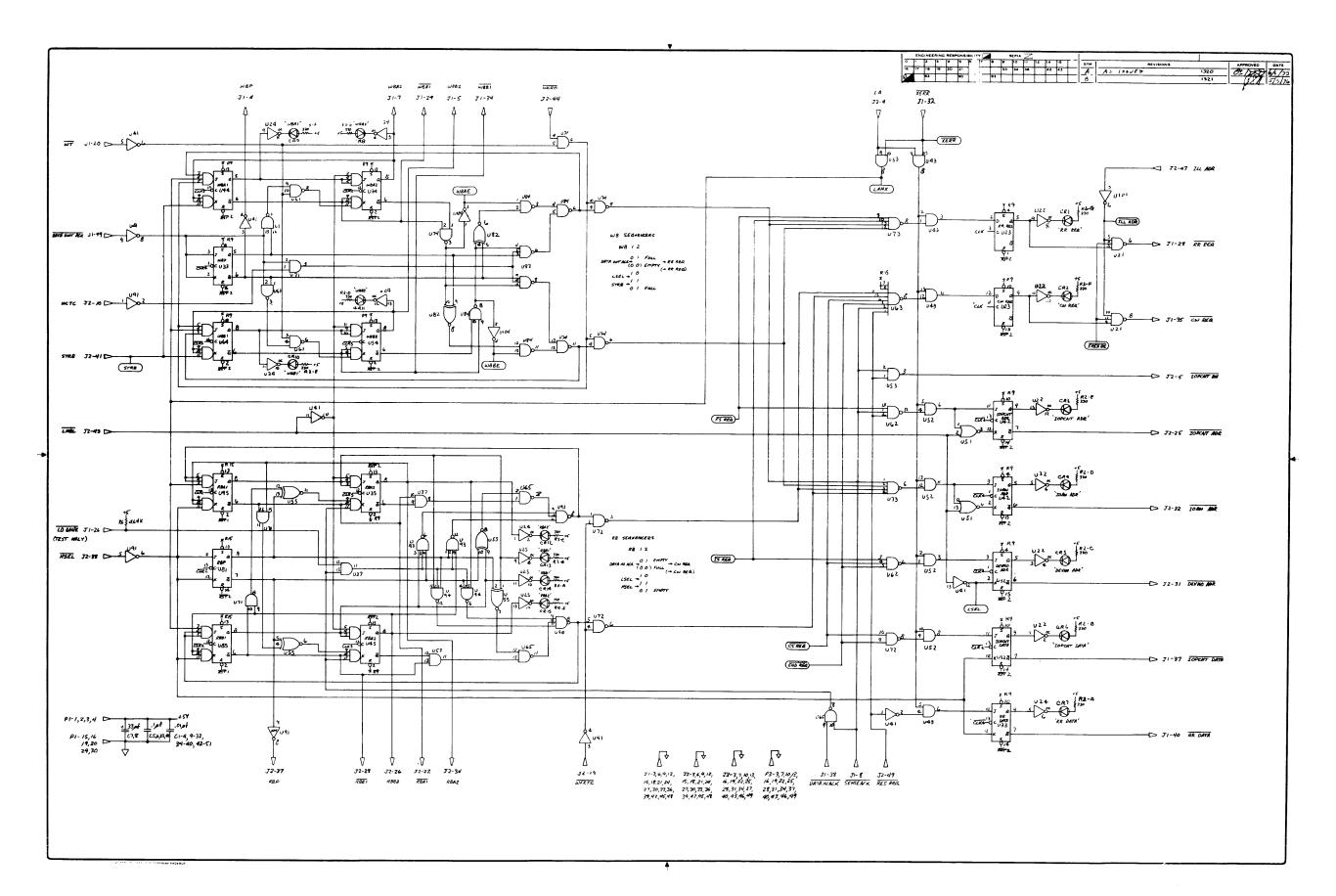


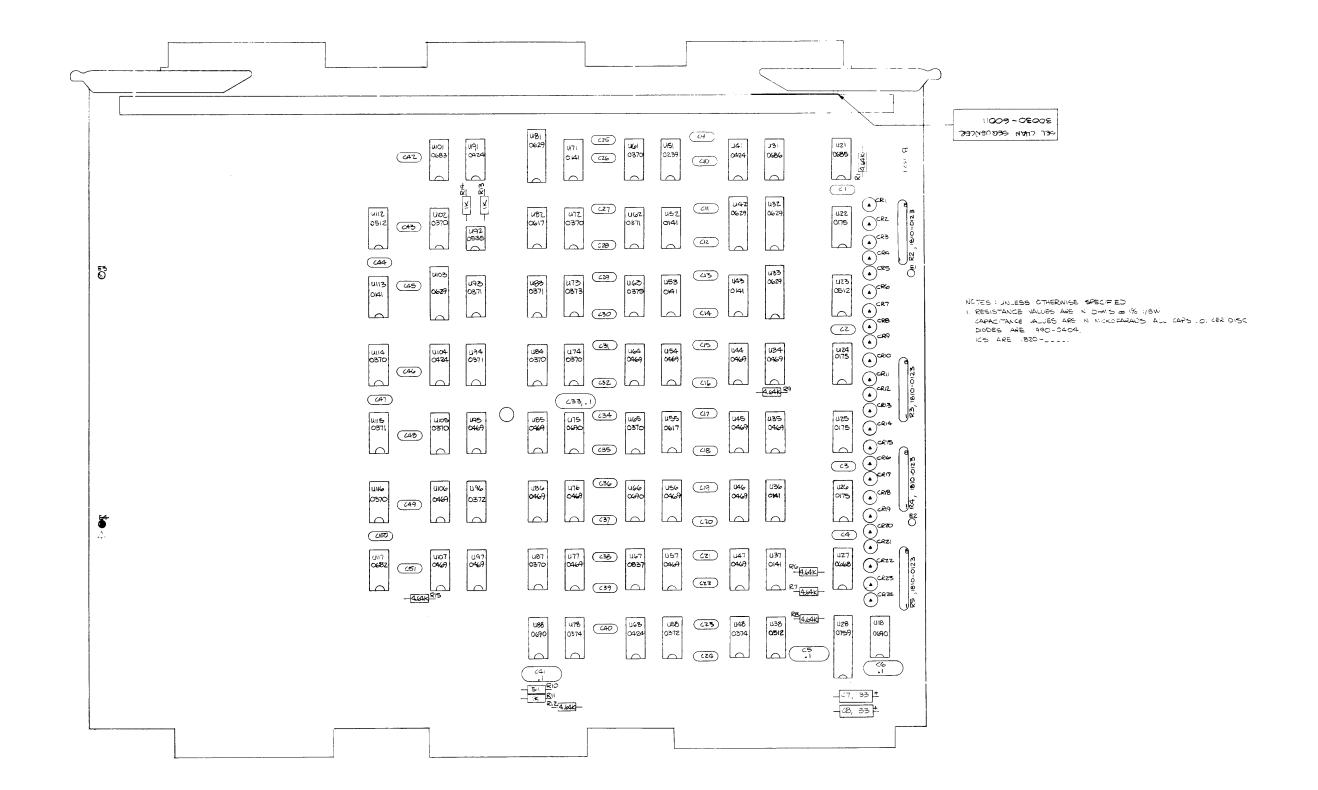


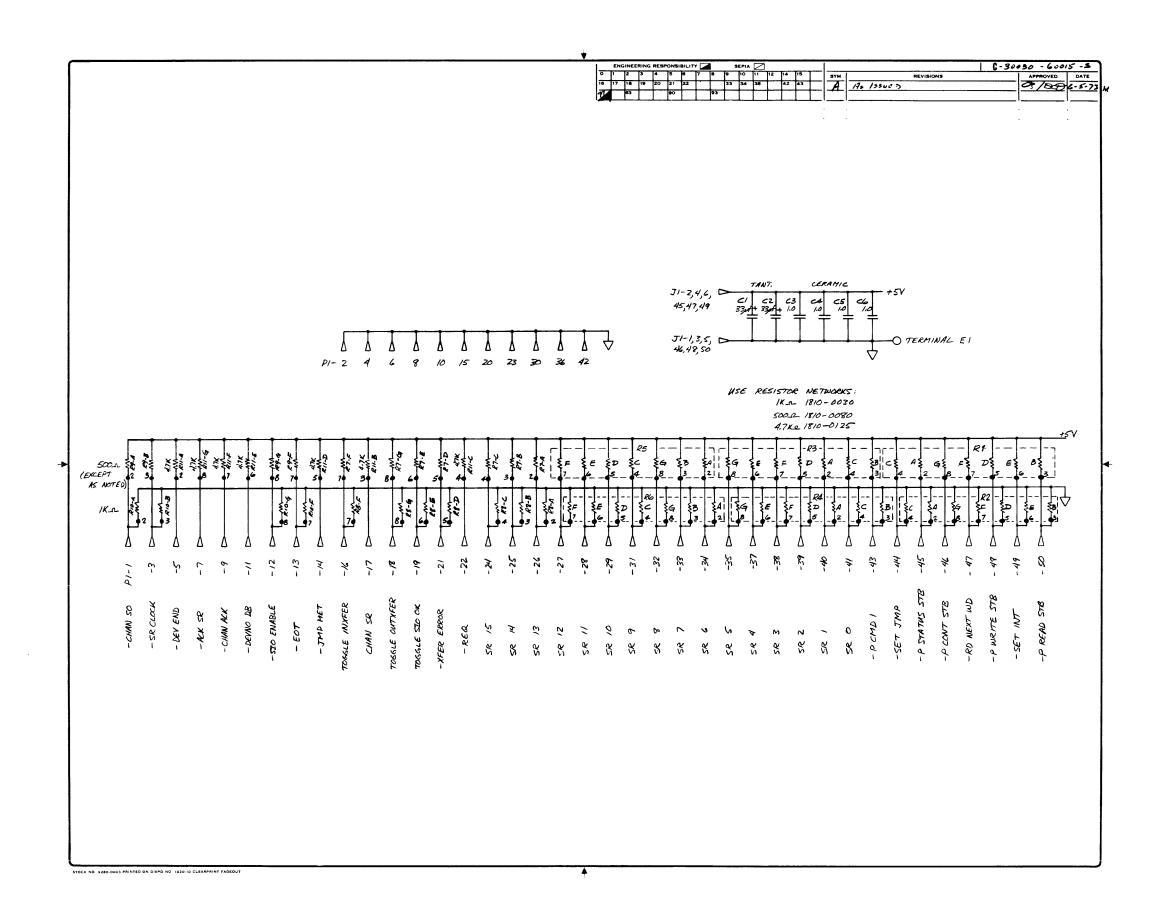


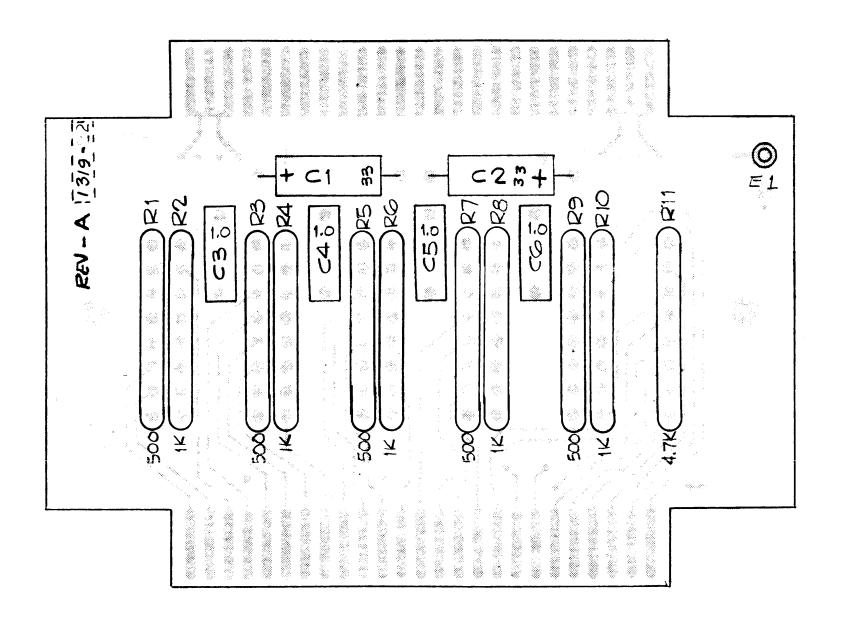






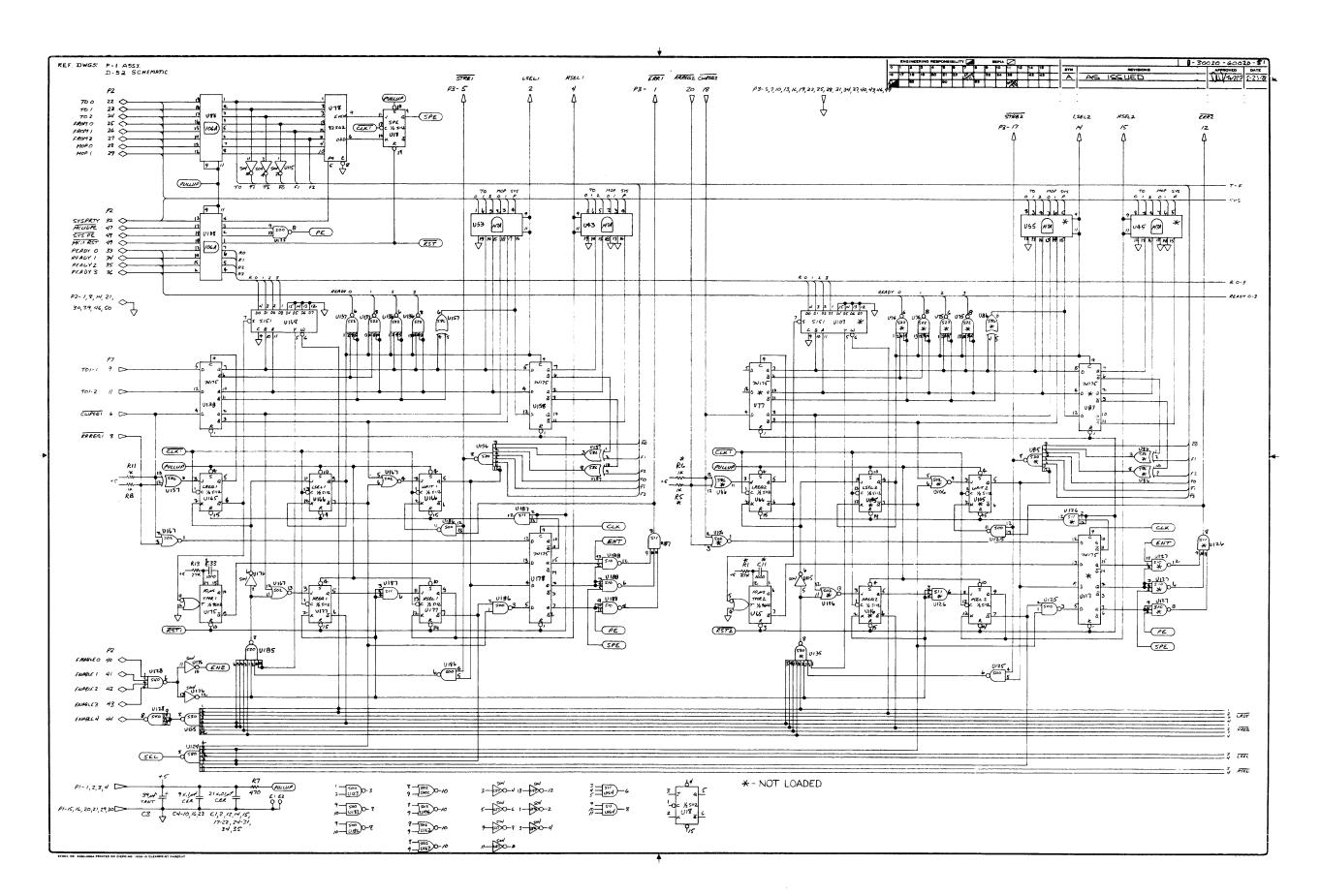


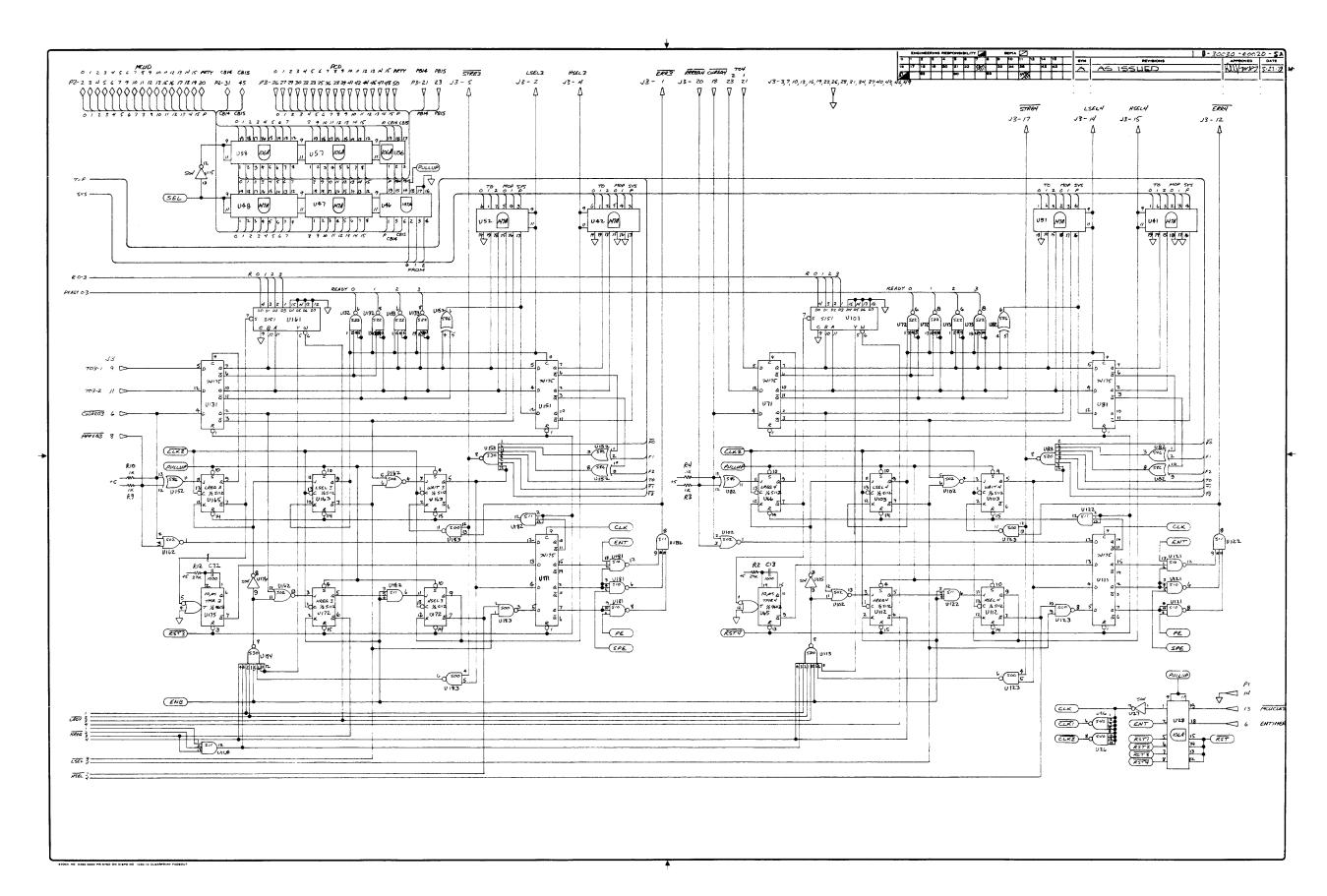


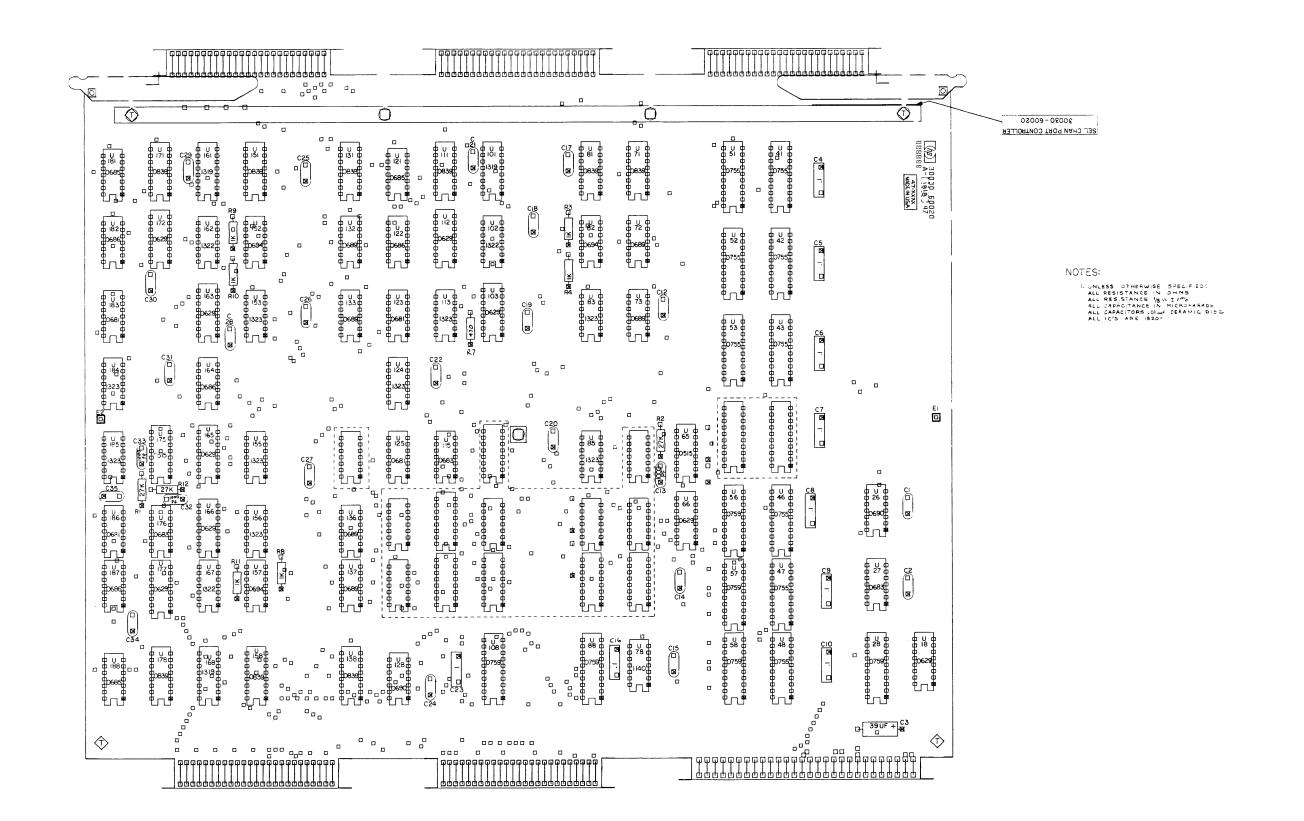


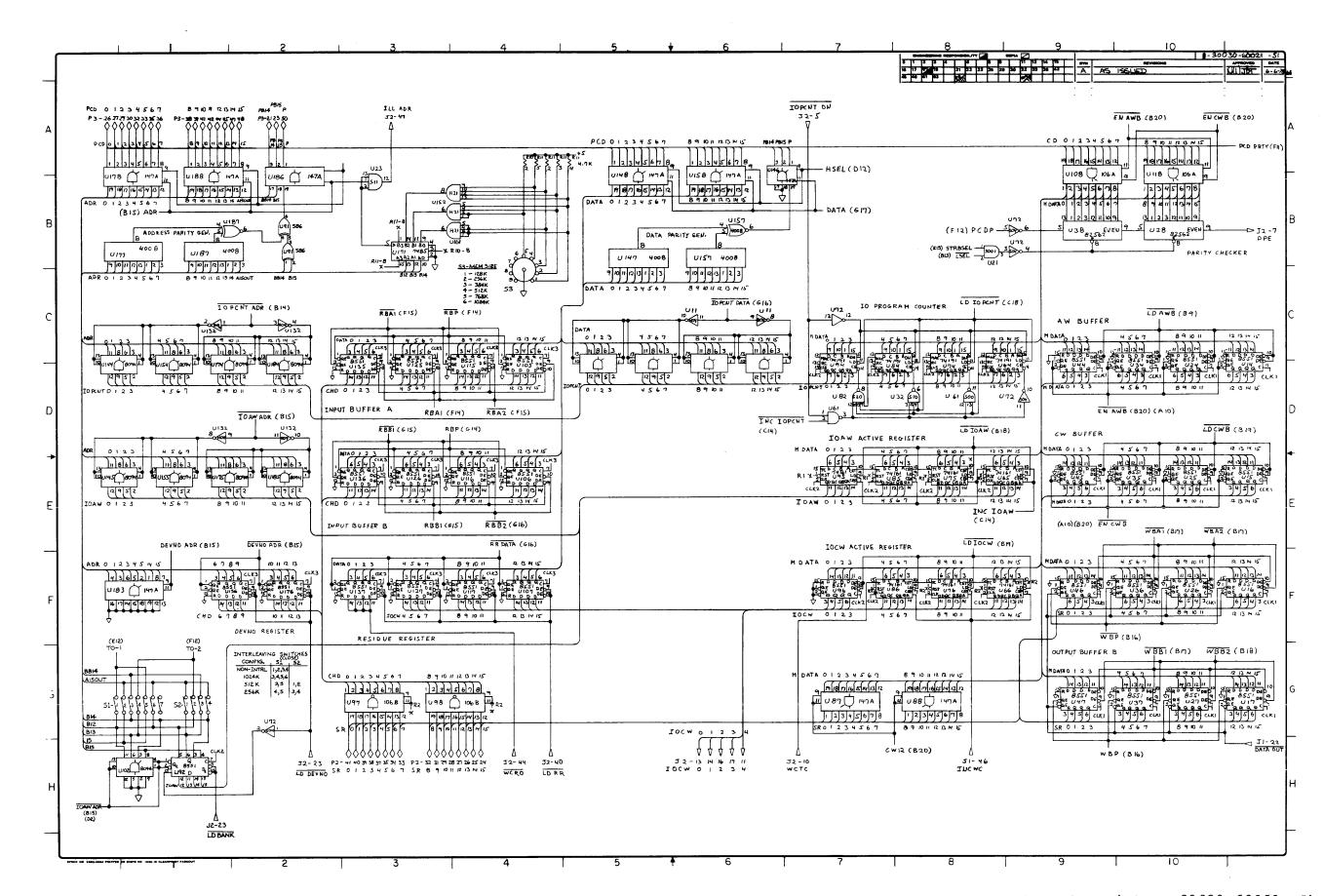
NOTES :

1. UNLESS OTHERWISE NOTED : ALL RESISTANCE IN OHMS ALL CAPACITANCE IN MICROFARADS

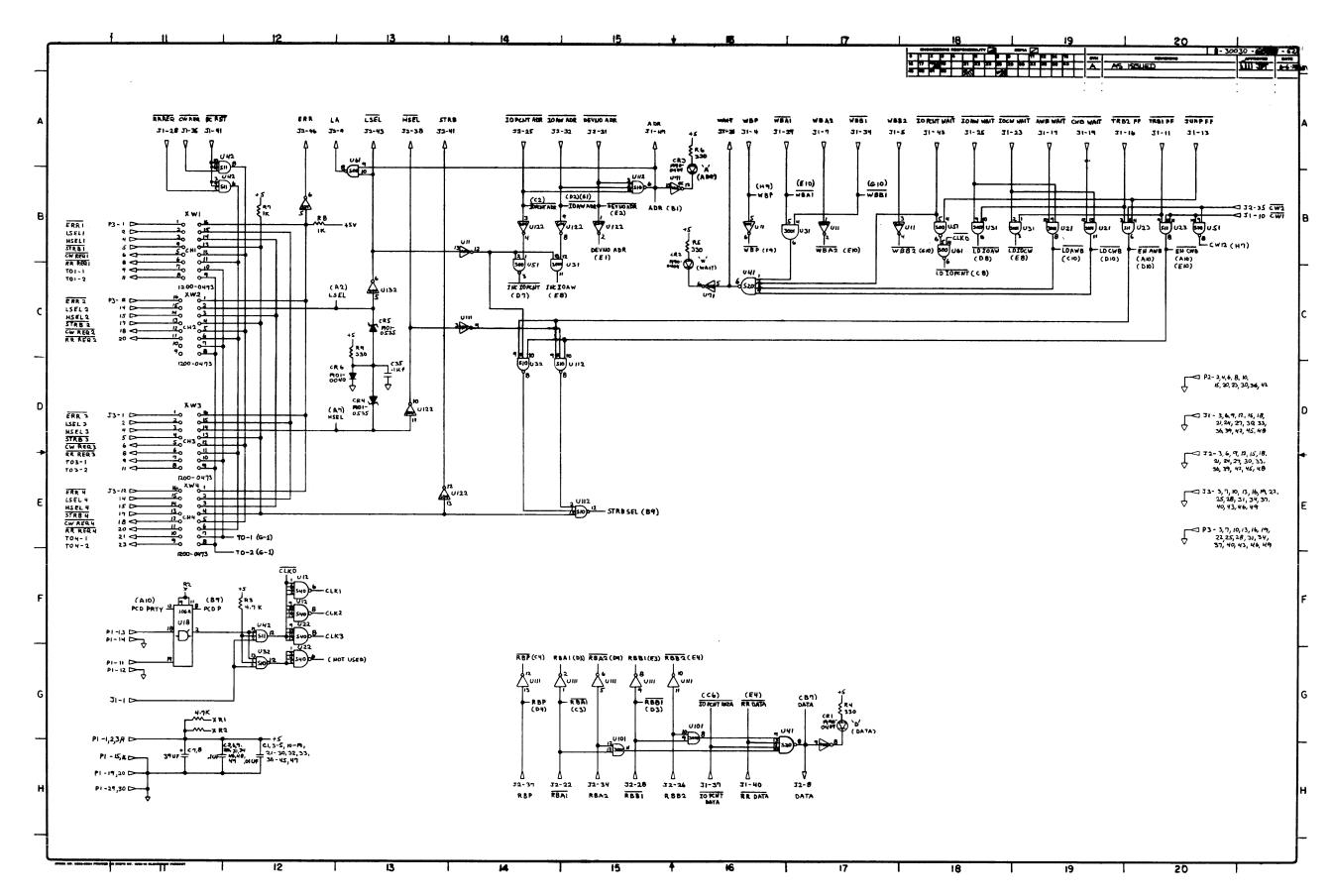


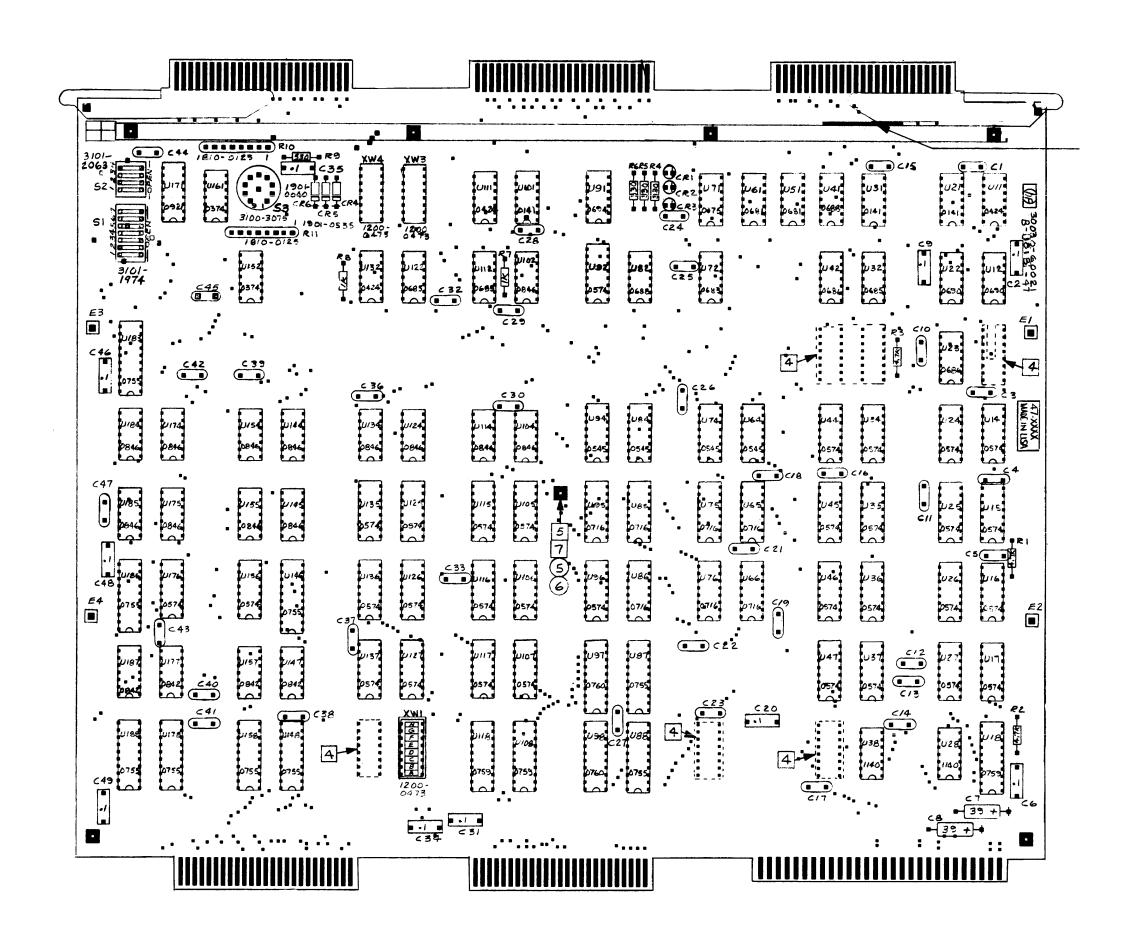


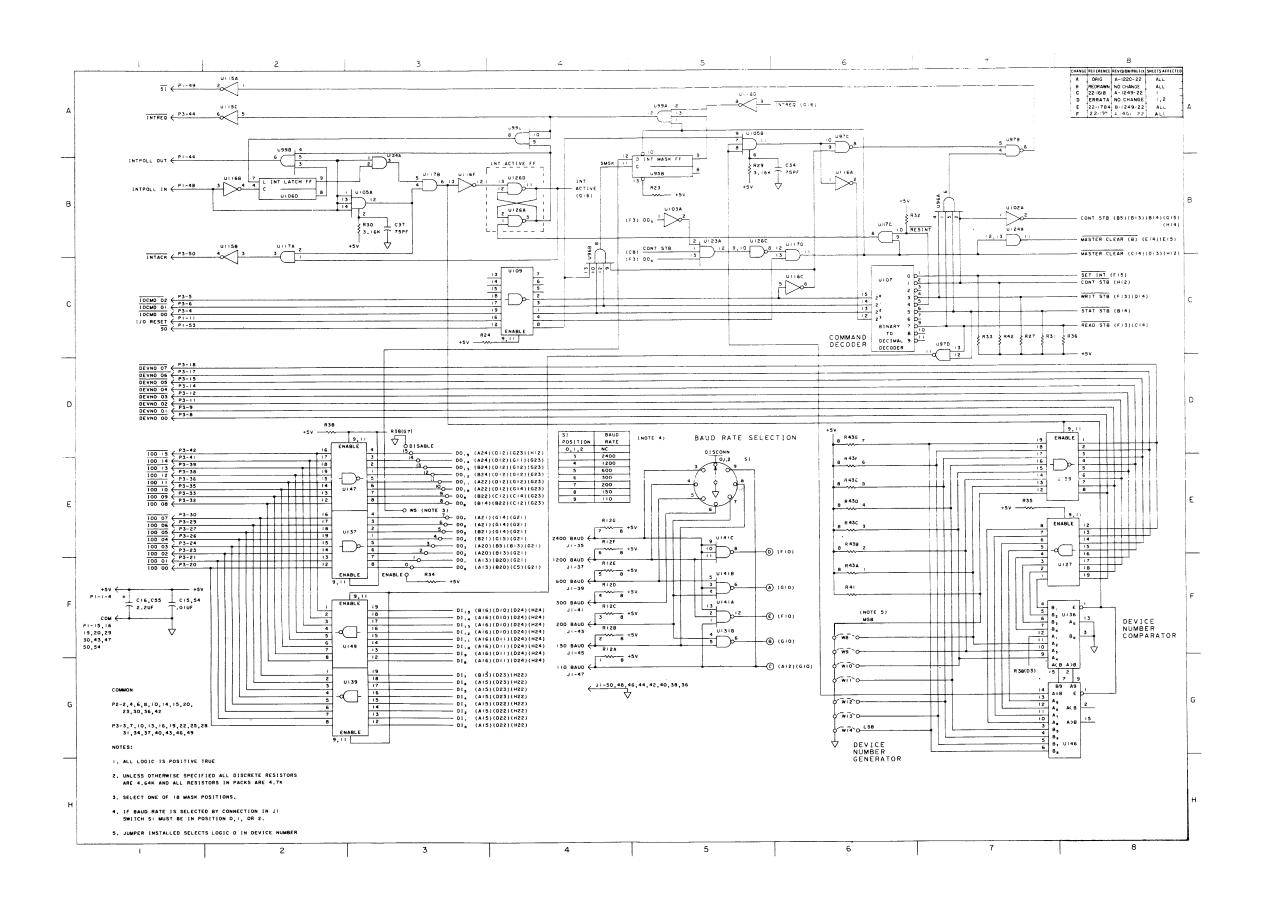


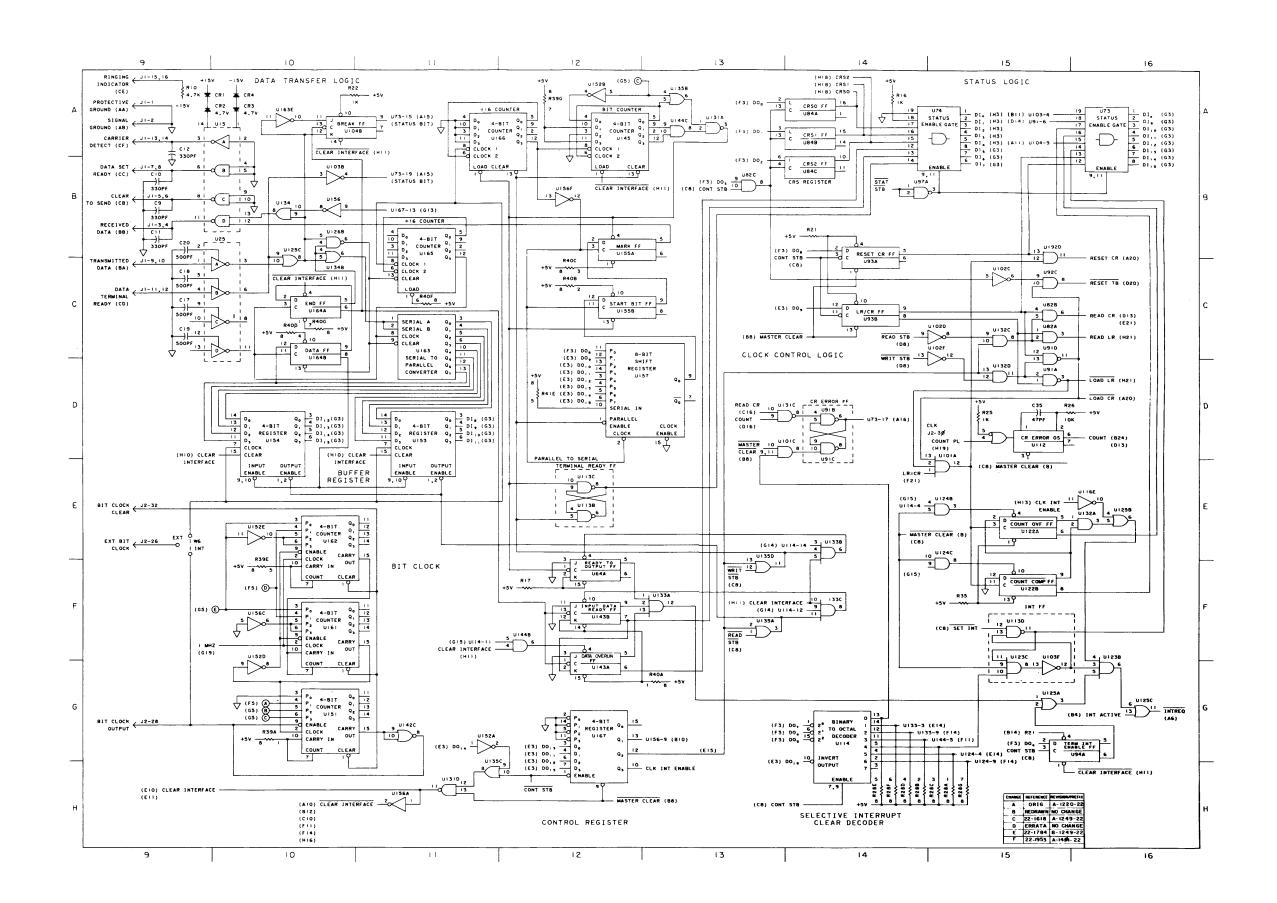


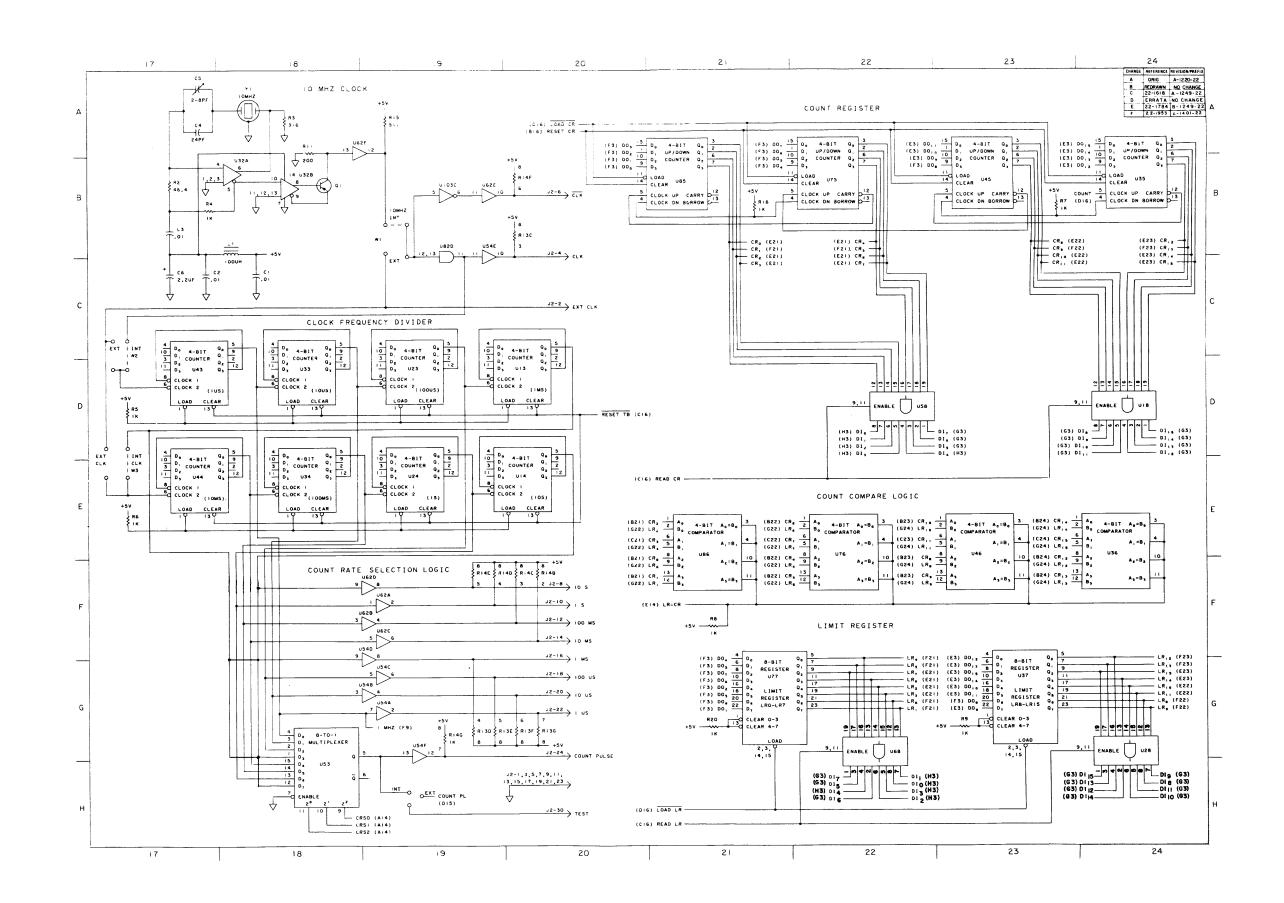
Selector Channel Register, 30030-60021, Sheet 1 of 3

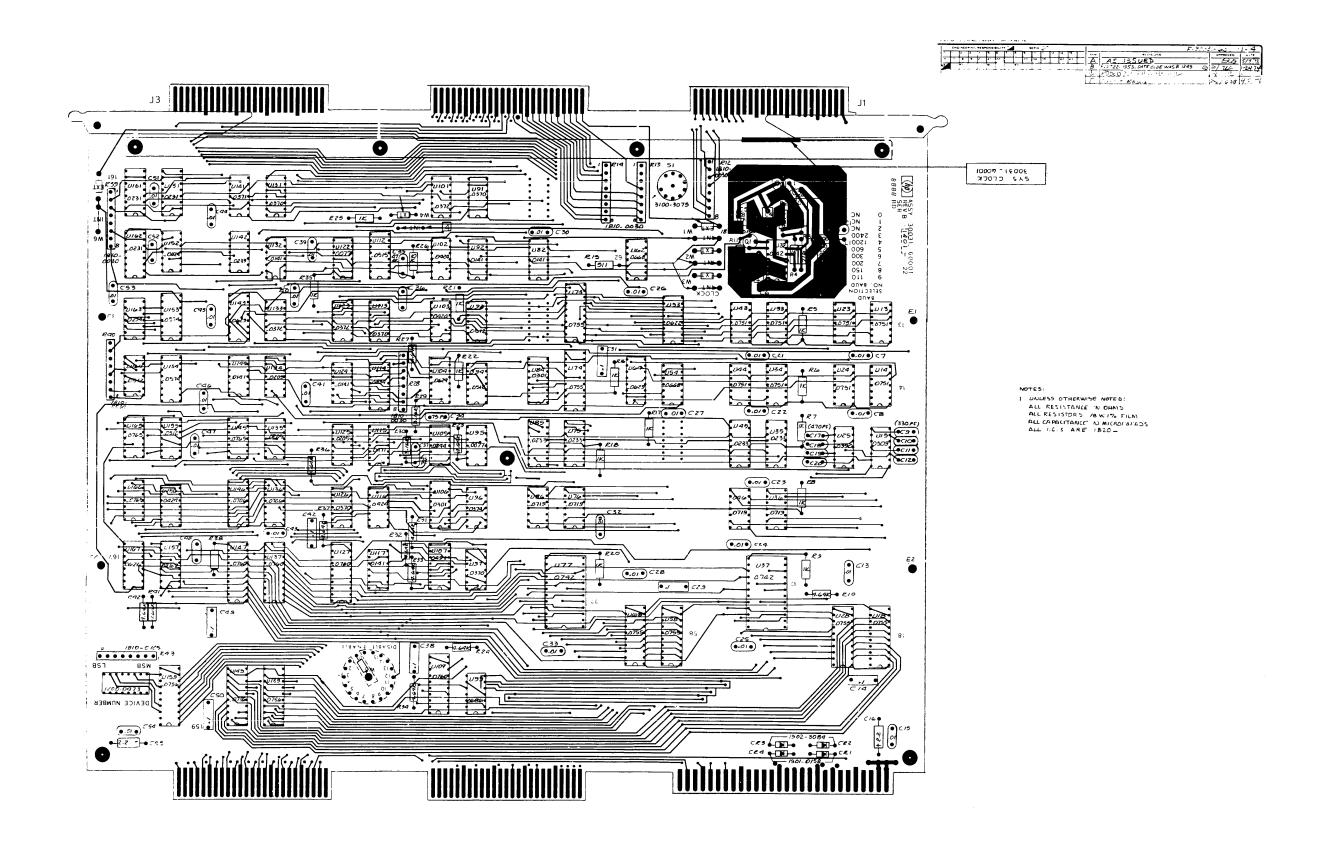


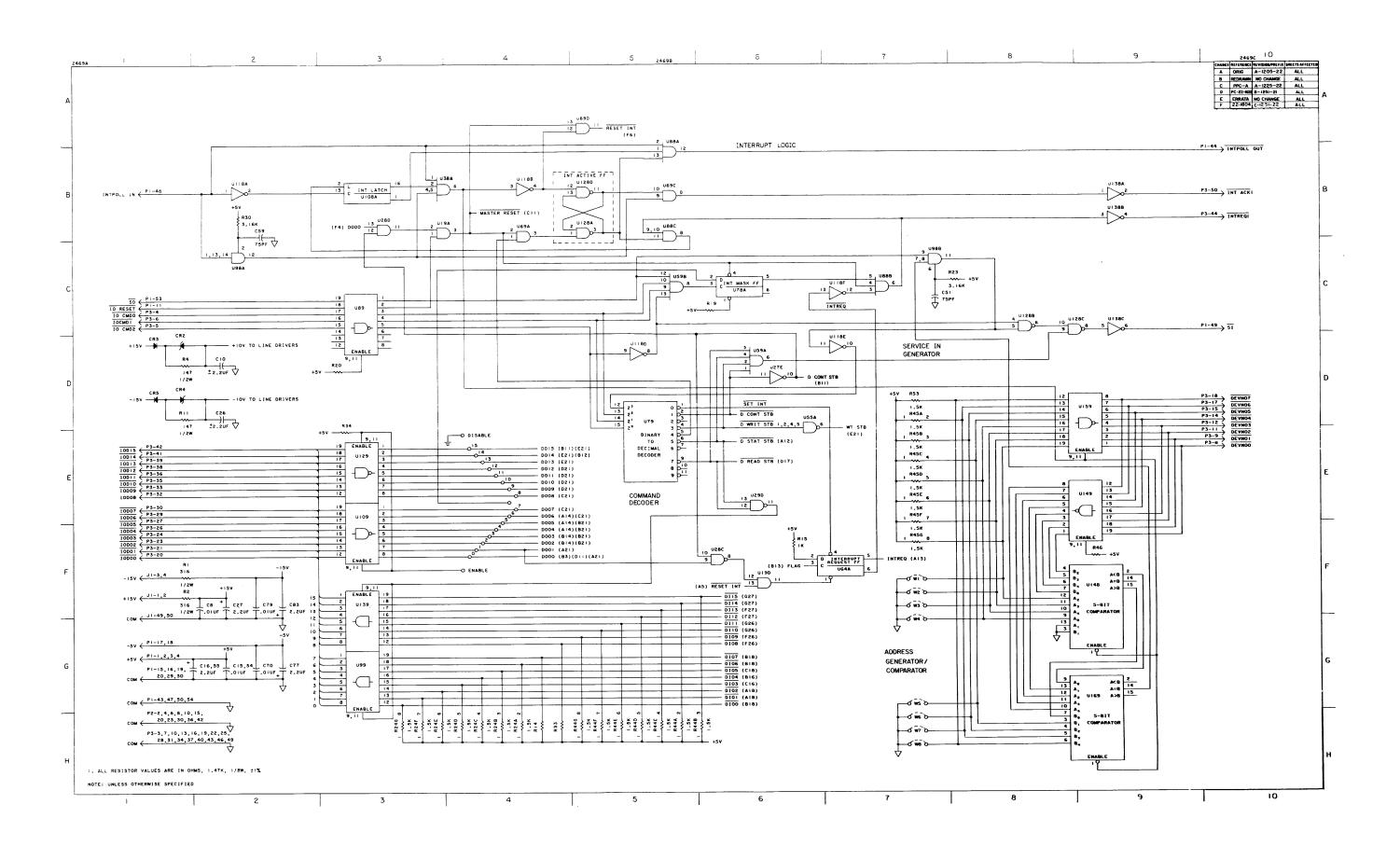


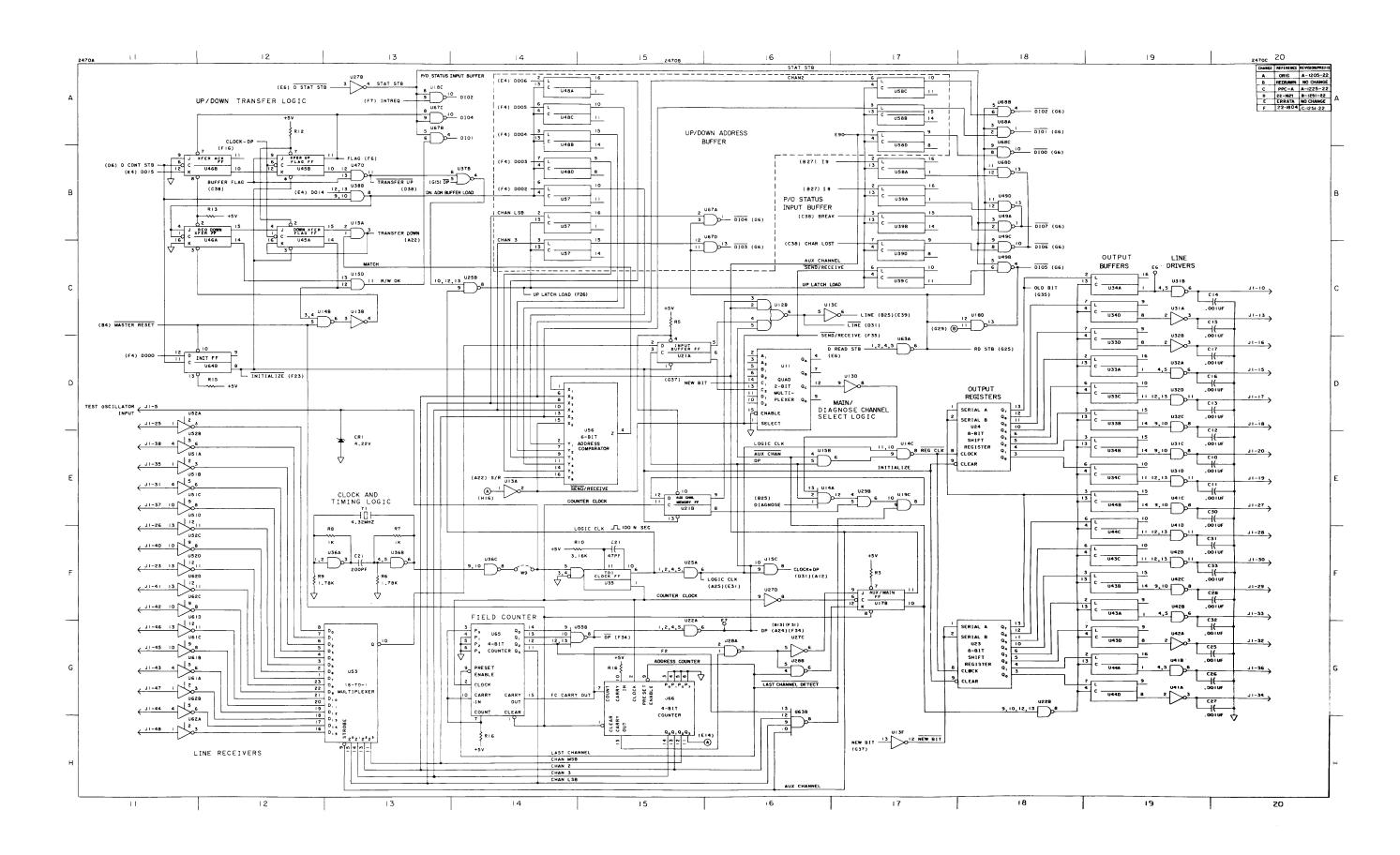


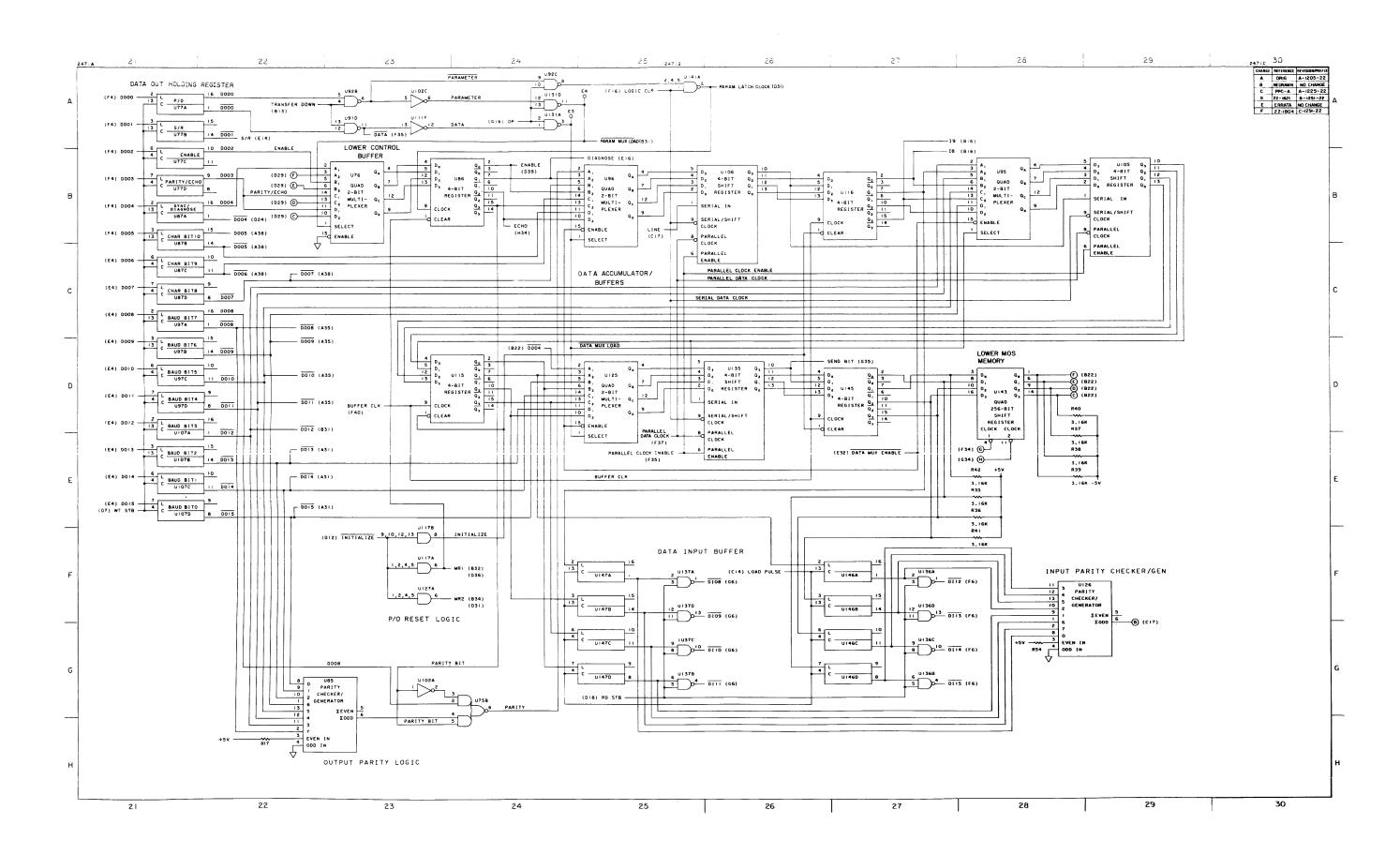


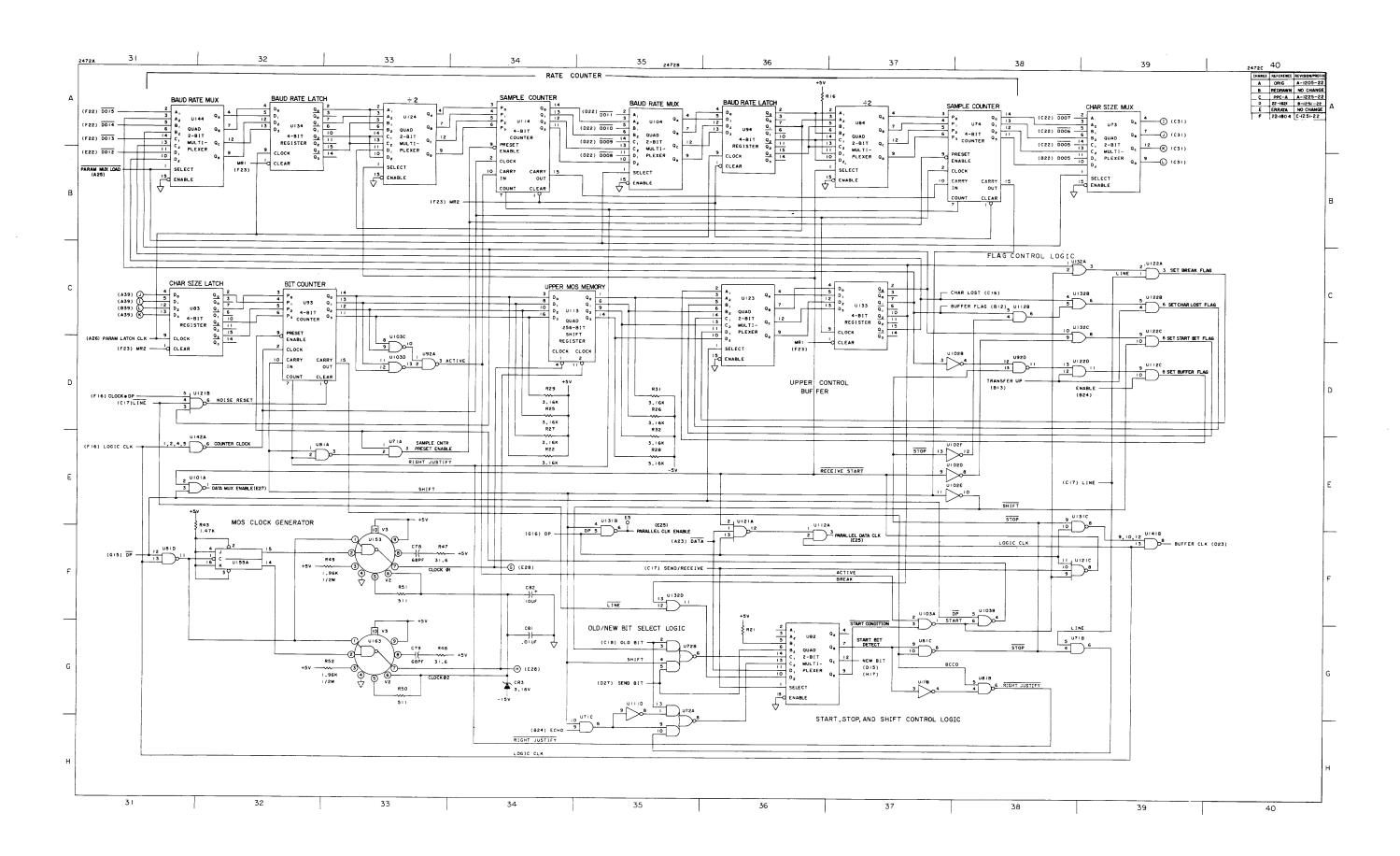


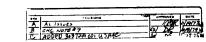


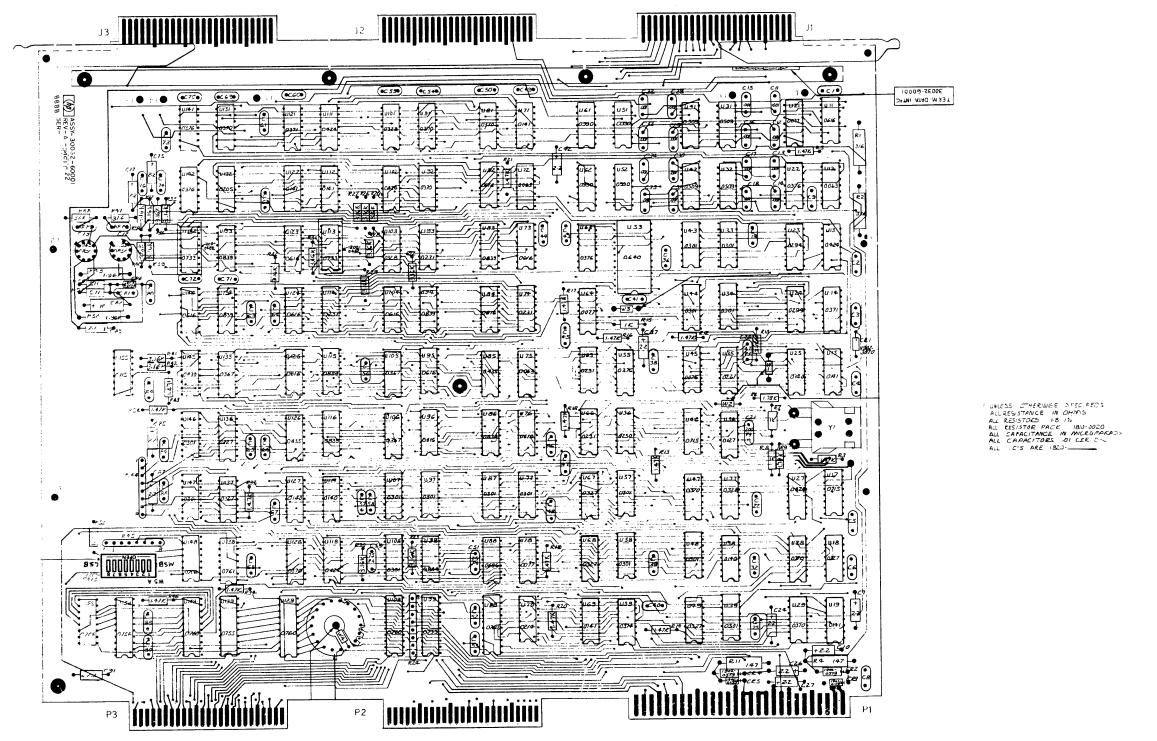


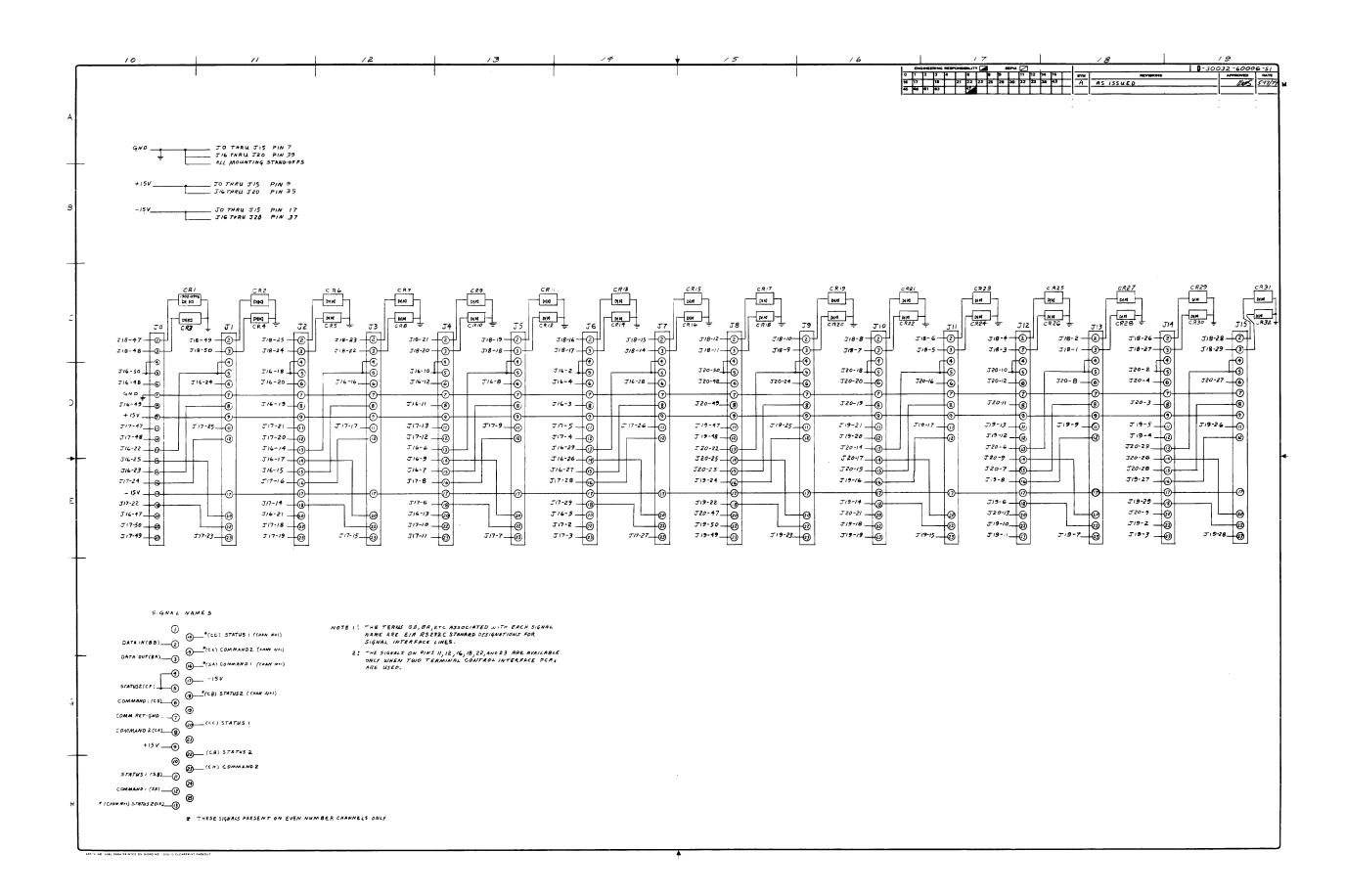


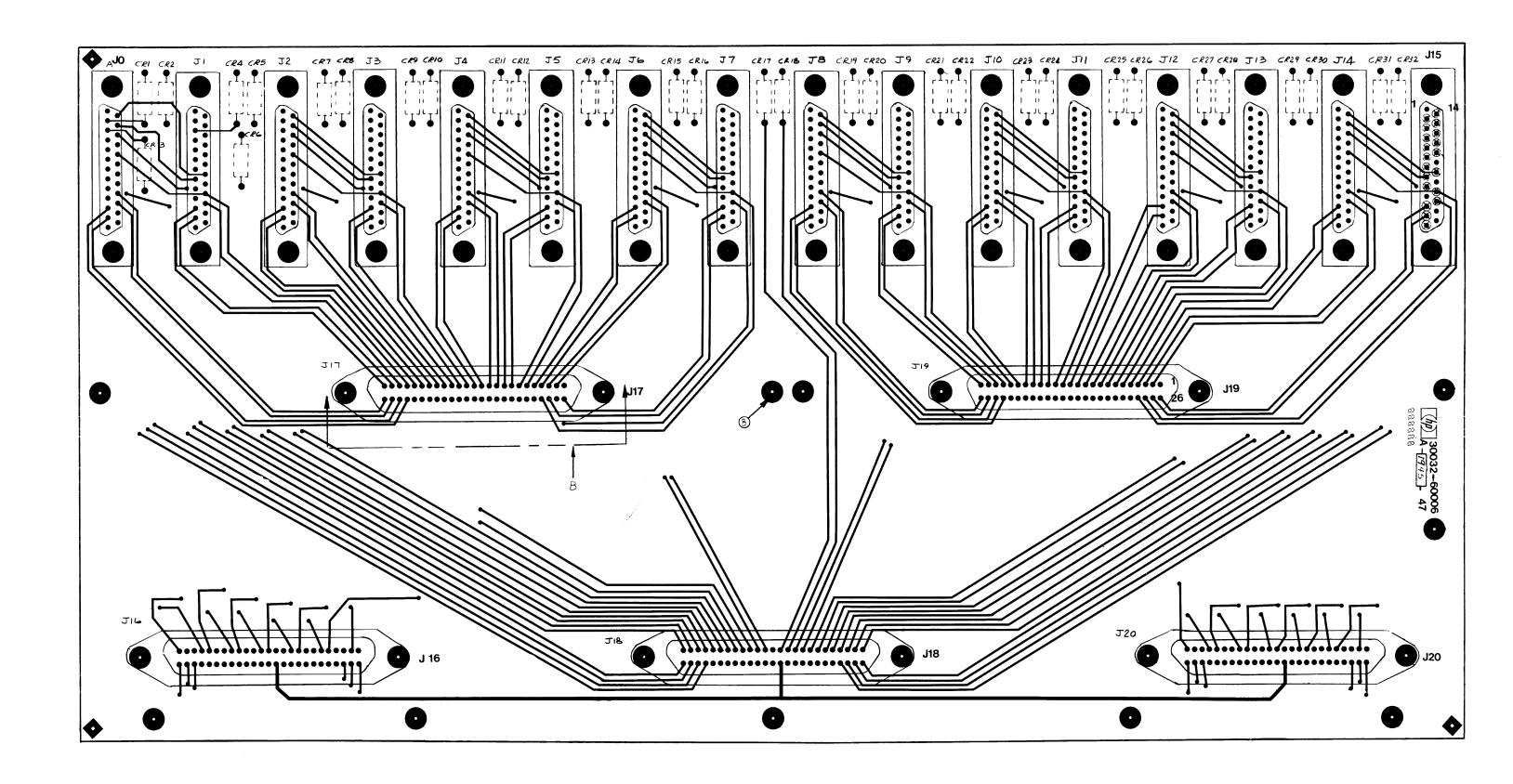


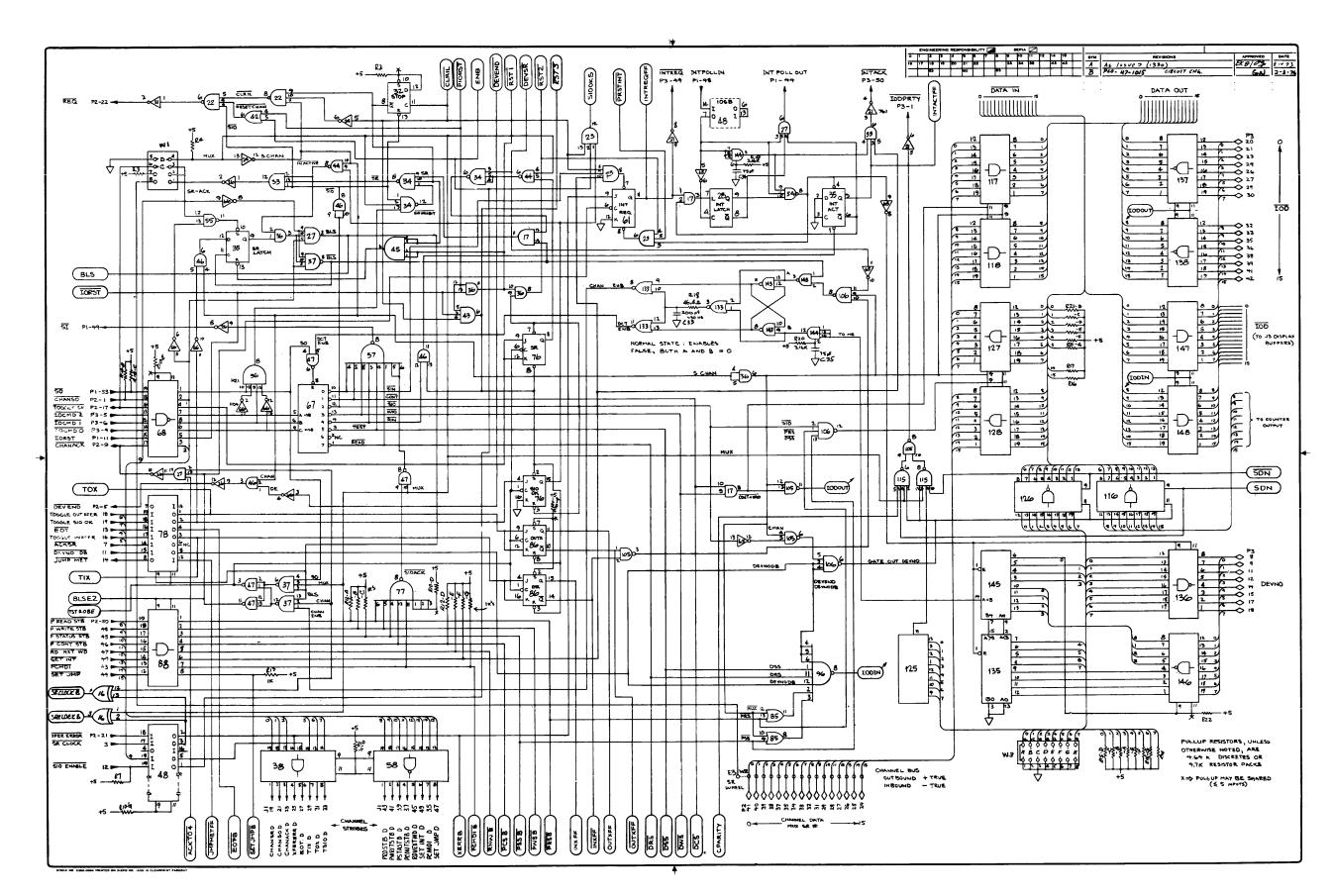


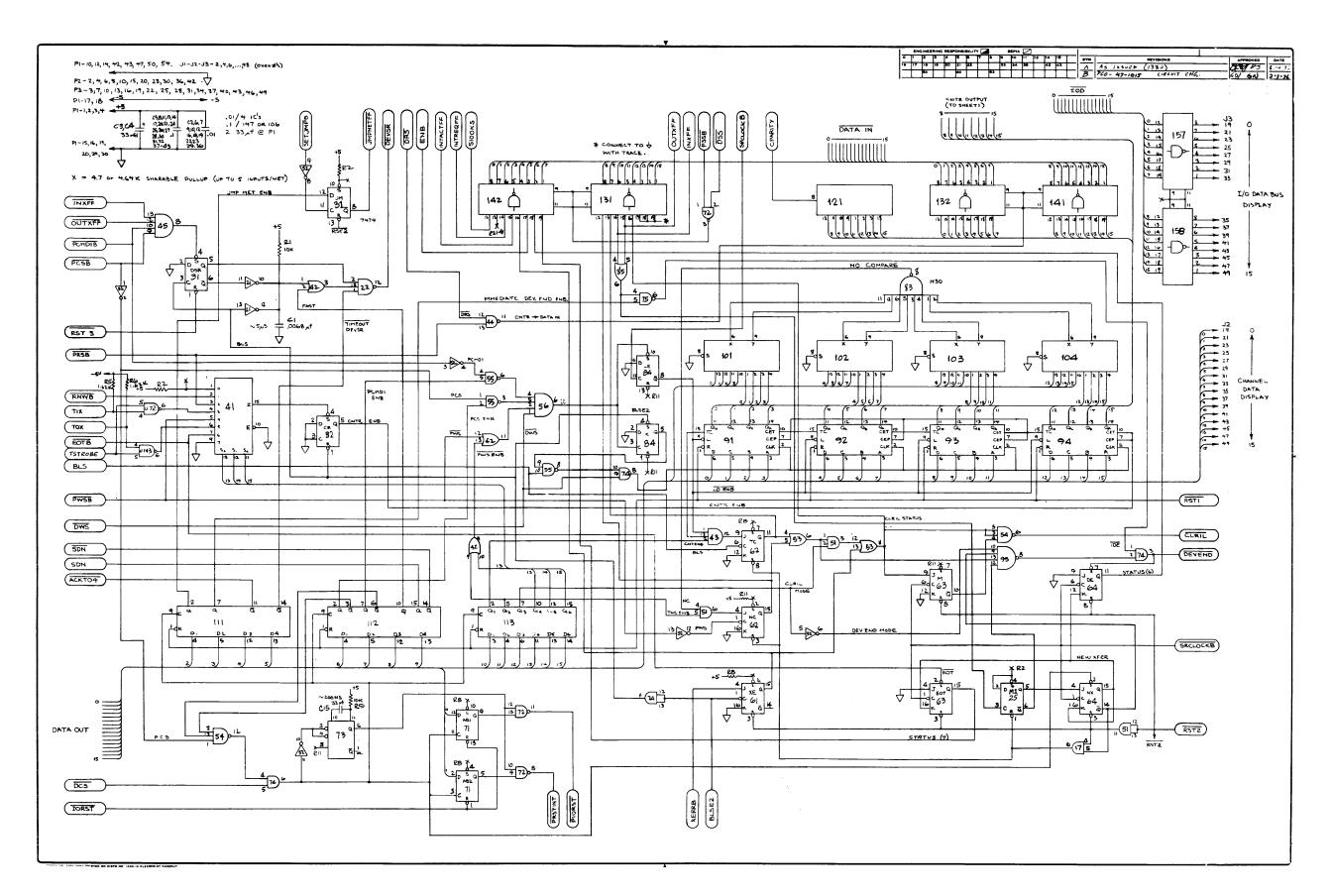


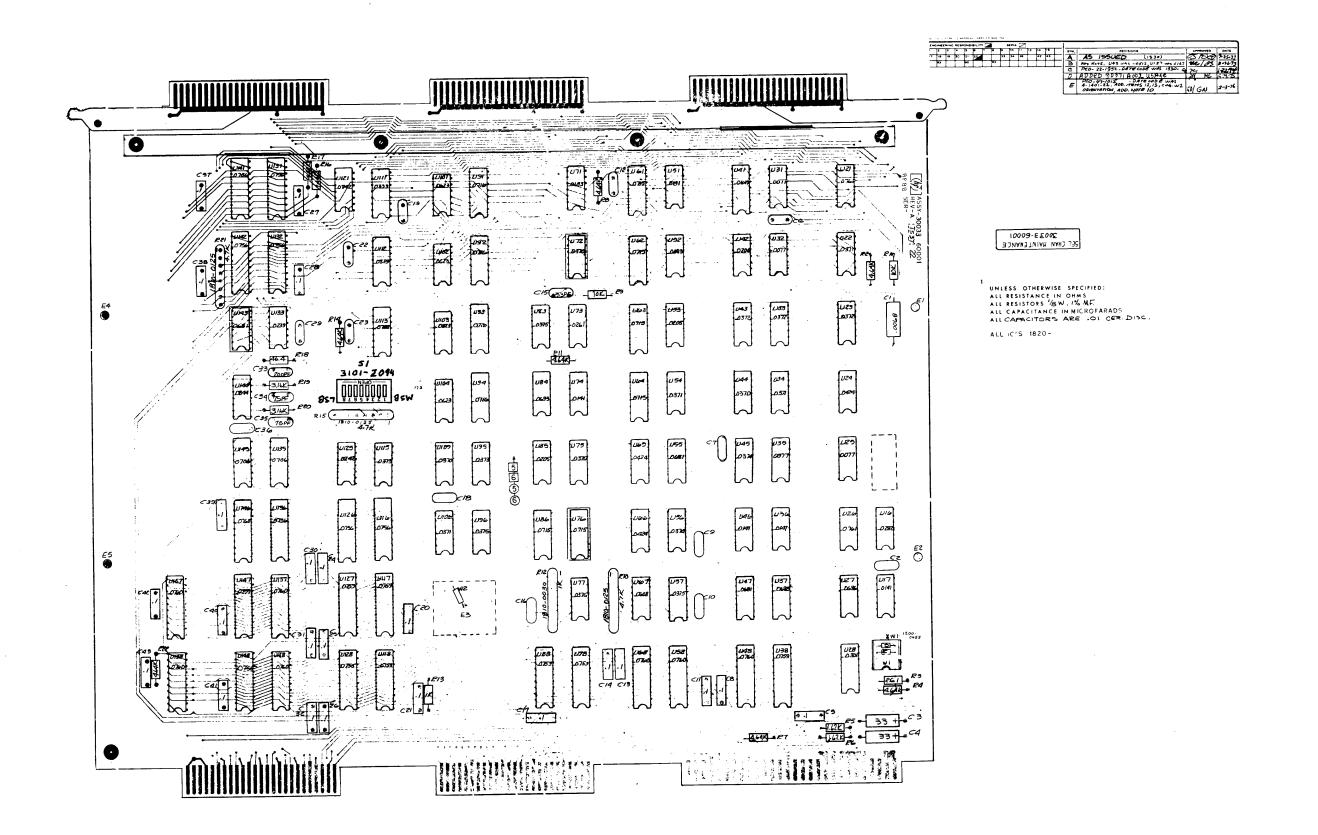


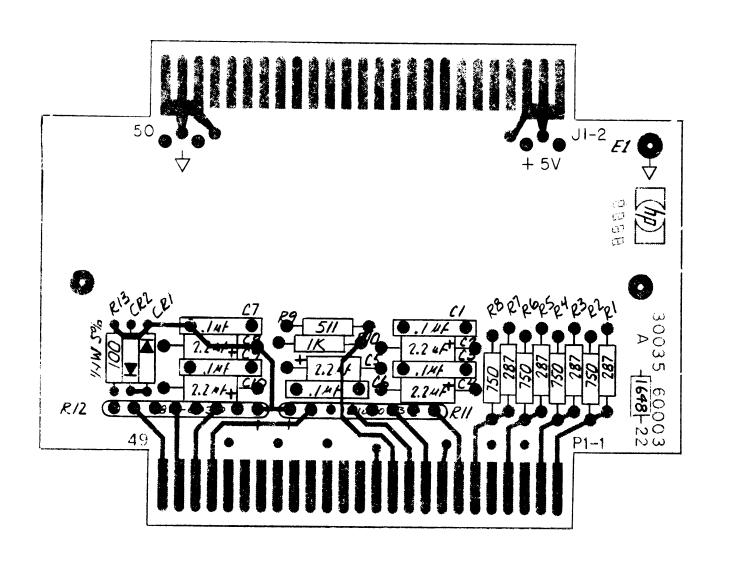












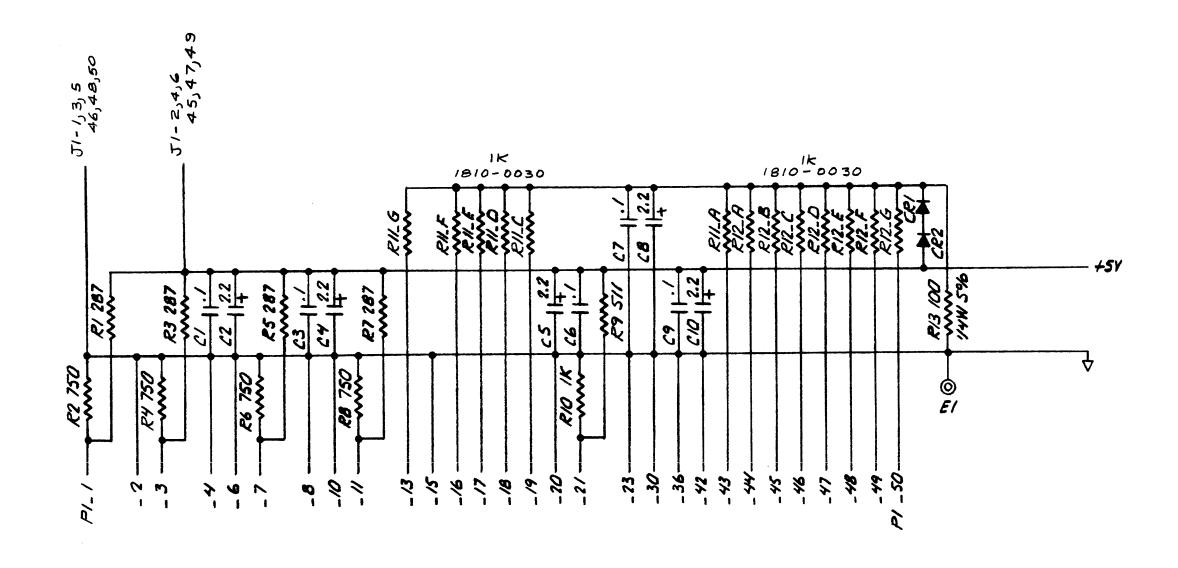
1. LINLESS OTHERWISE NOTED

PLL RESISTANCE IN OHMS

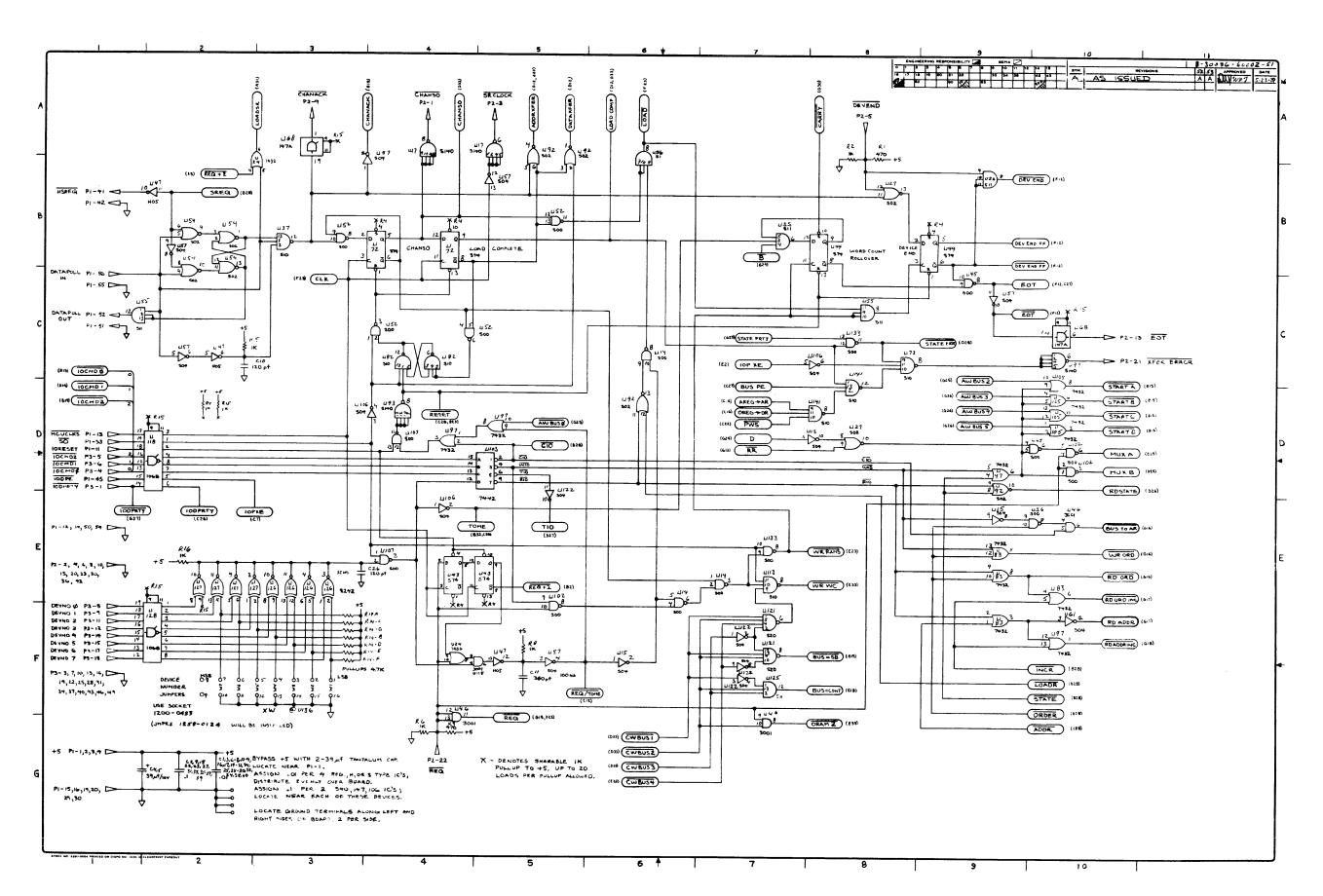
ALL RESISTORS IBW 1% M.F.

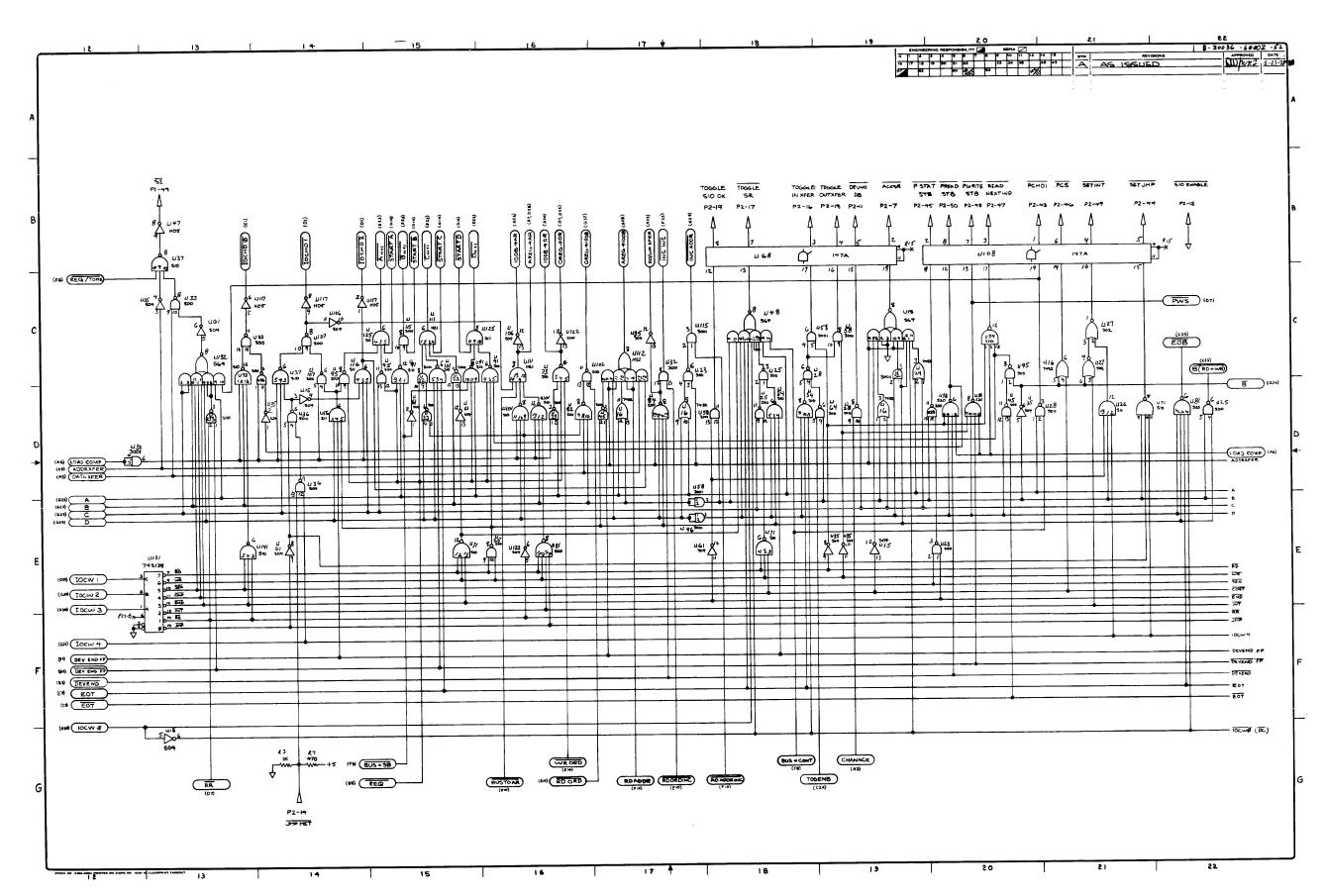
ALL CAPACITANCE IN MICRO-FARADS

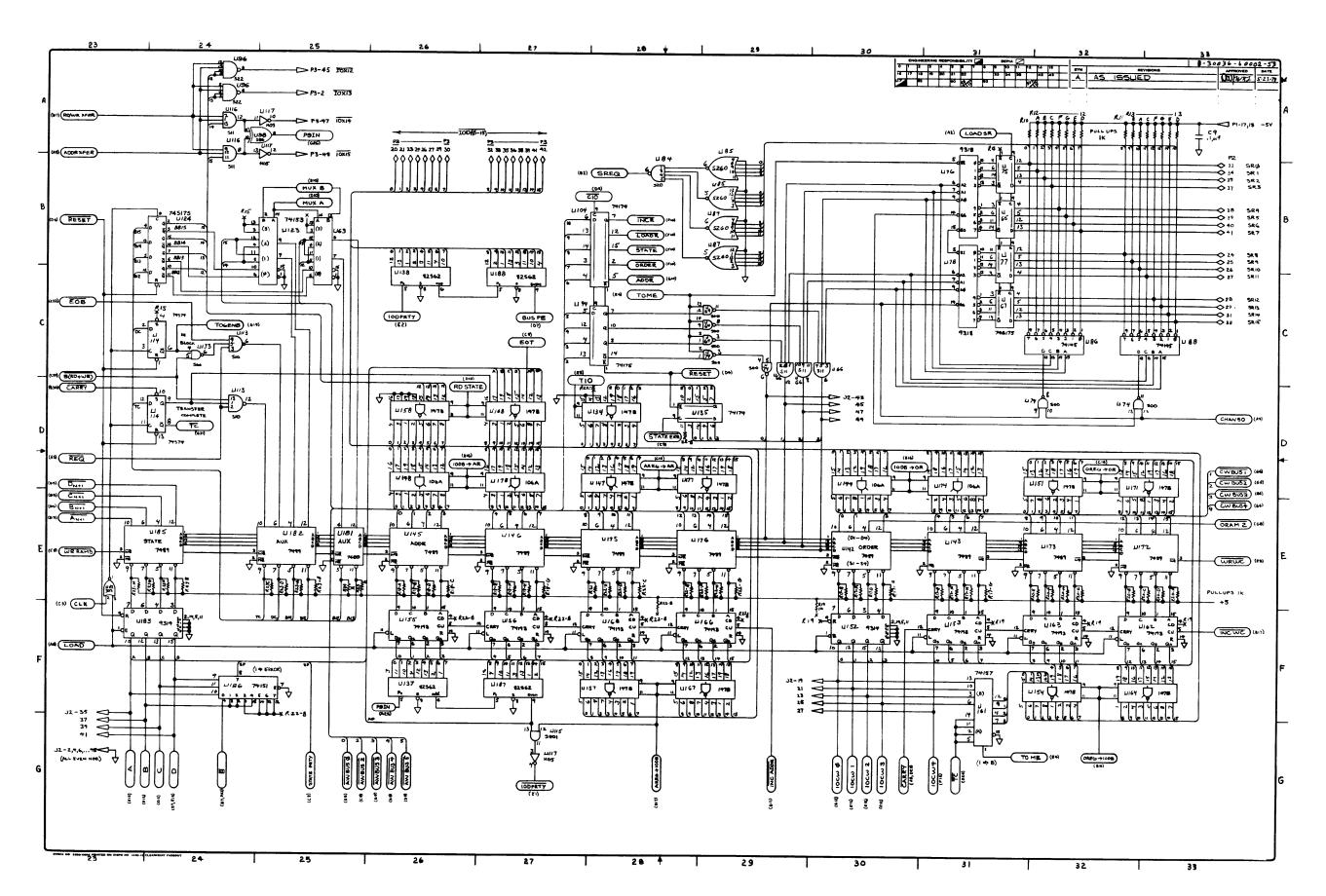
ALL DIODES #1901_0159

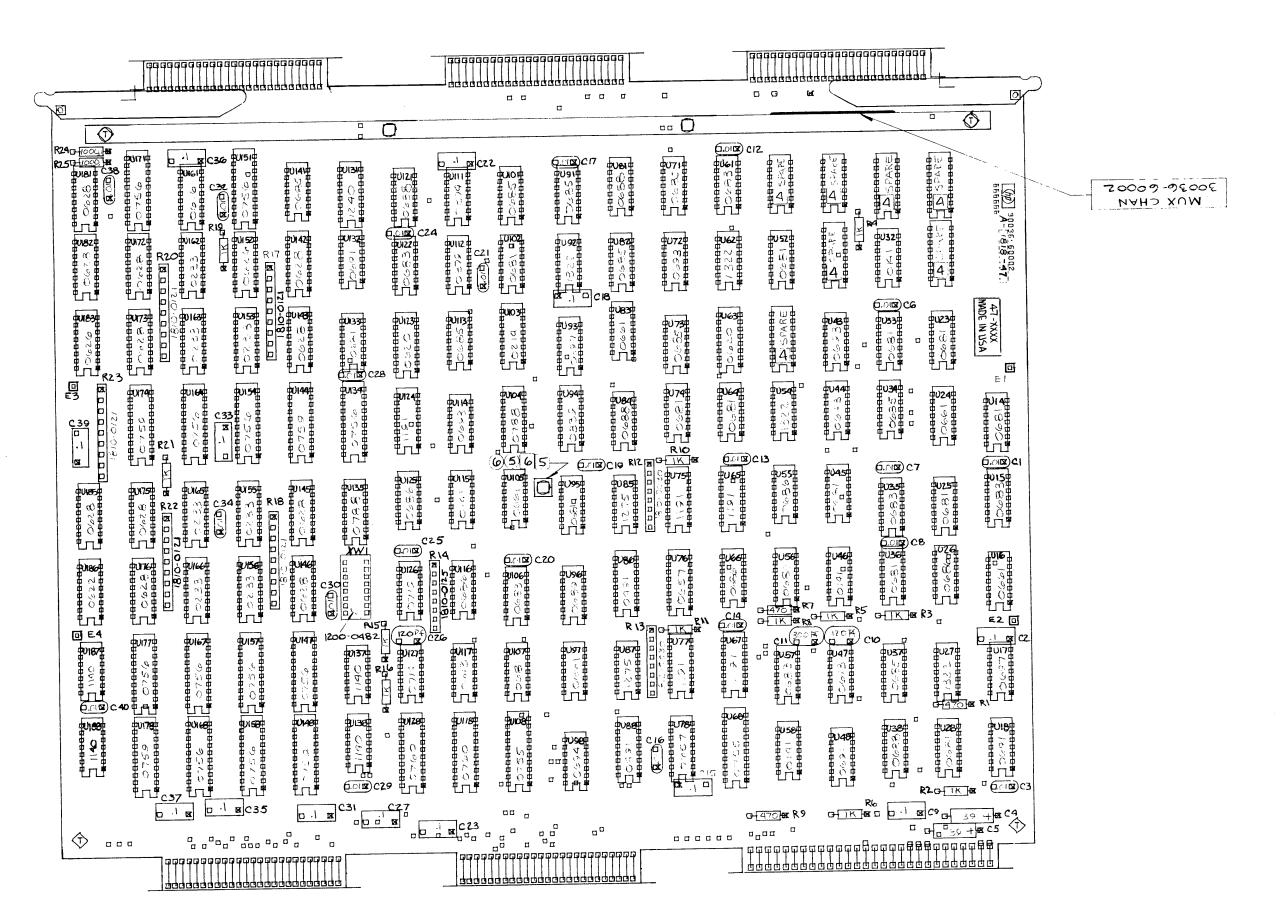


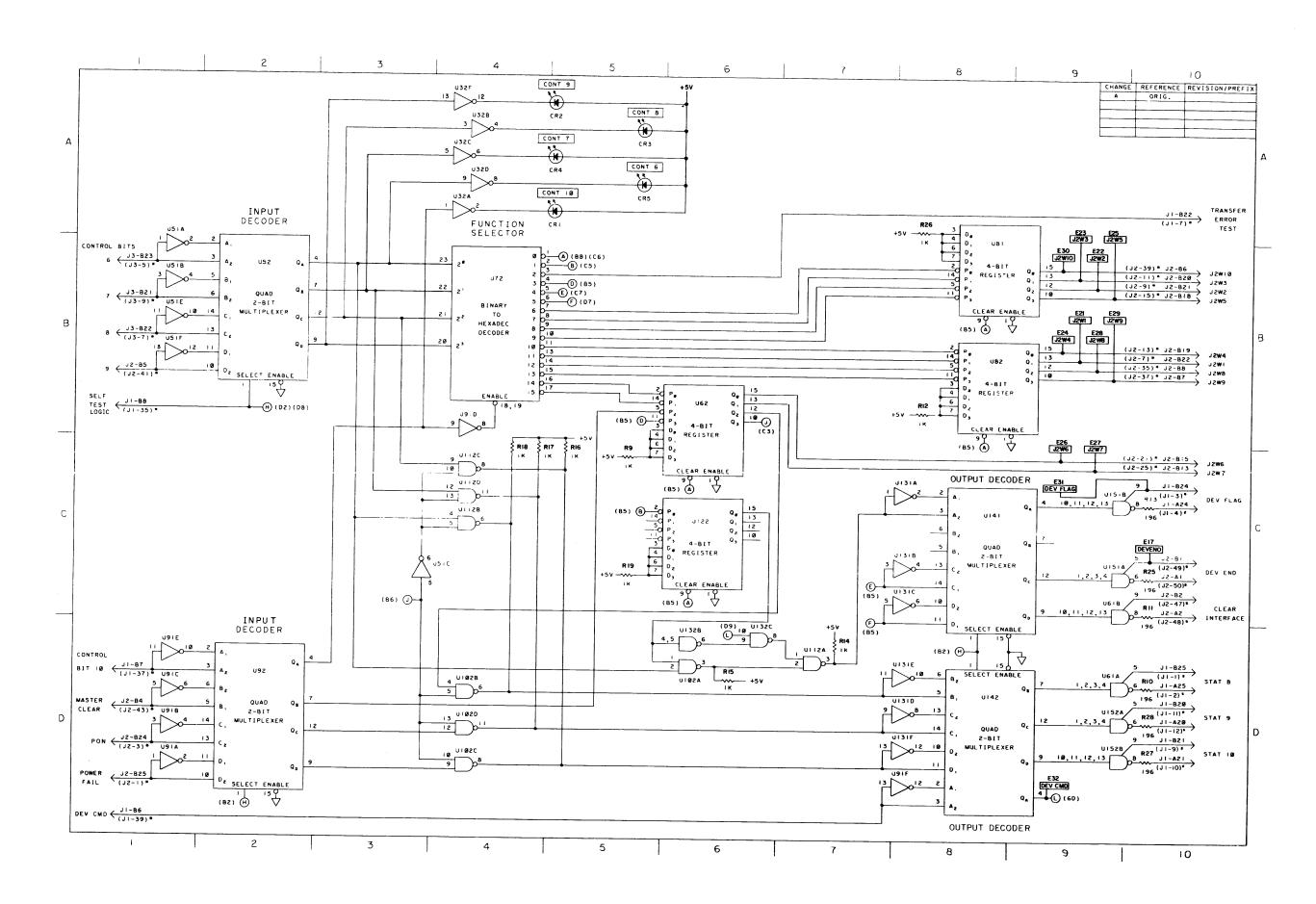
UNLESS OTHERWISE NOTED
ALL RESISTANCE IN OHMS
ALL RESISTORS YBW 1% MF
ALL CAPACITANCE IN MICRO FARADS
ALL DIODES #1901_0159



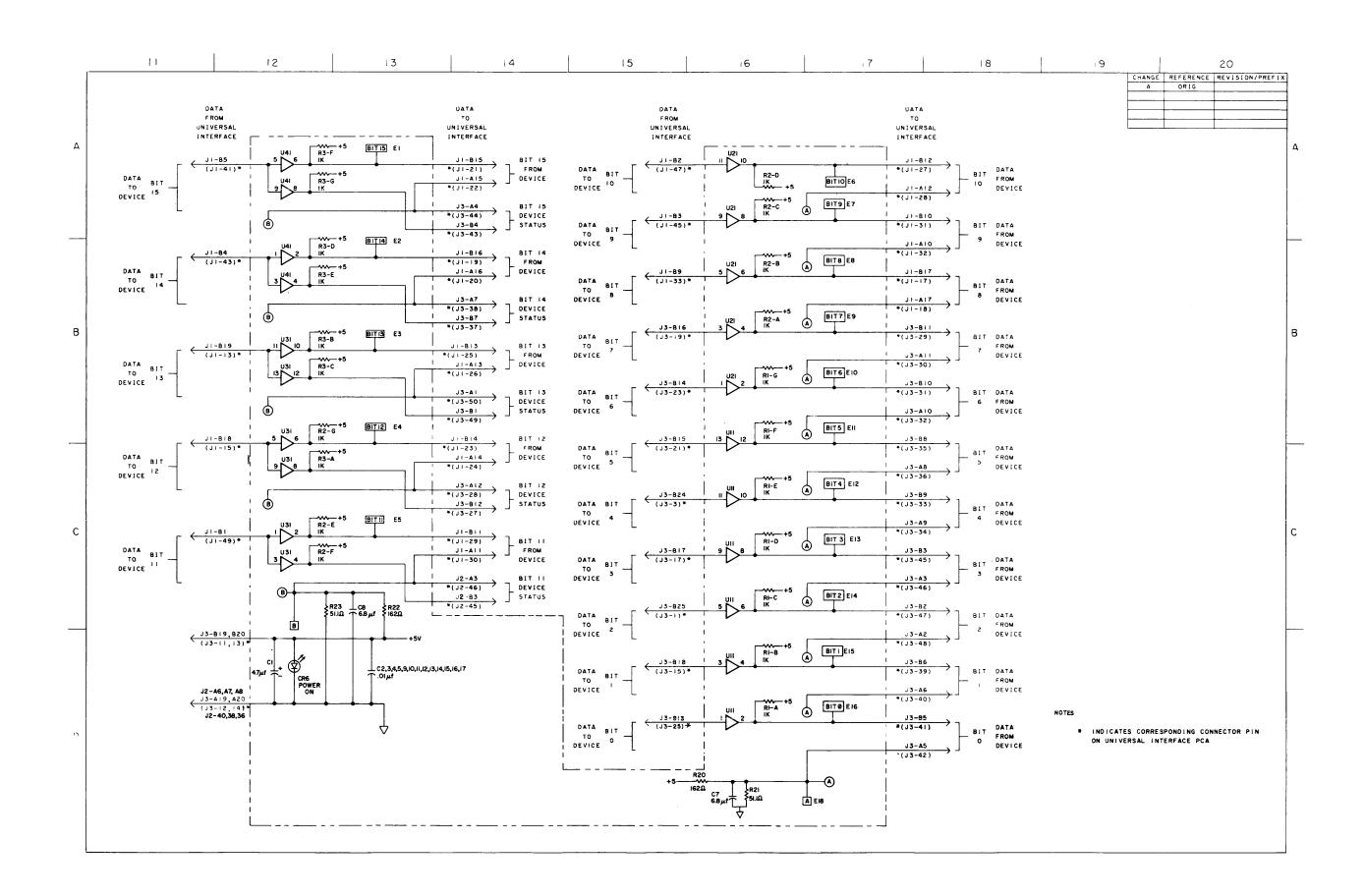




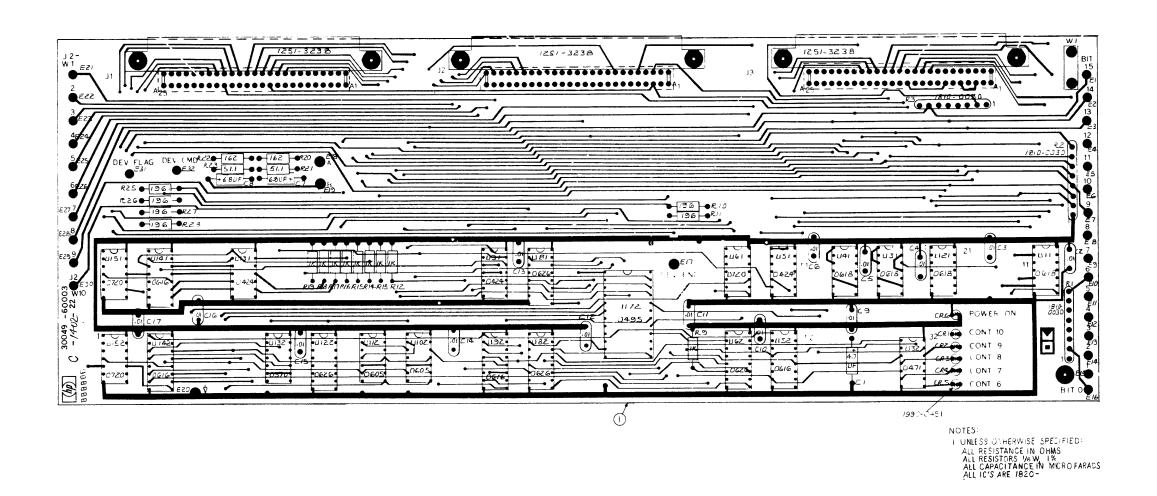


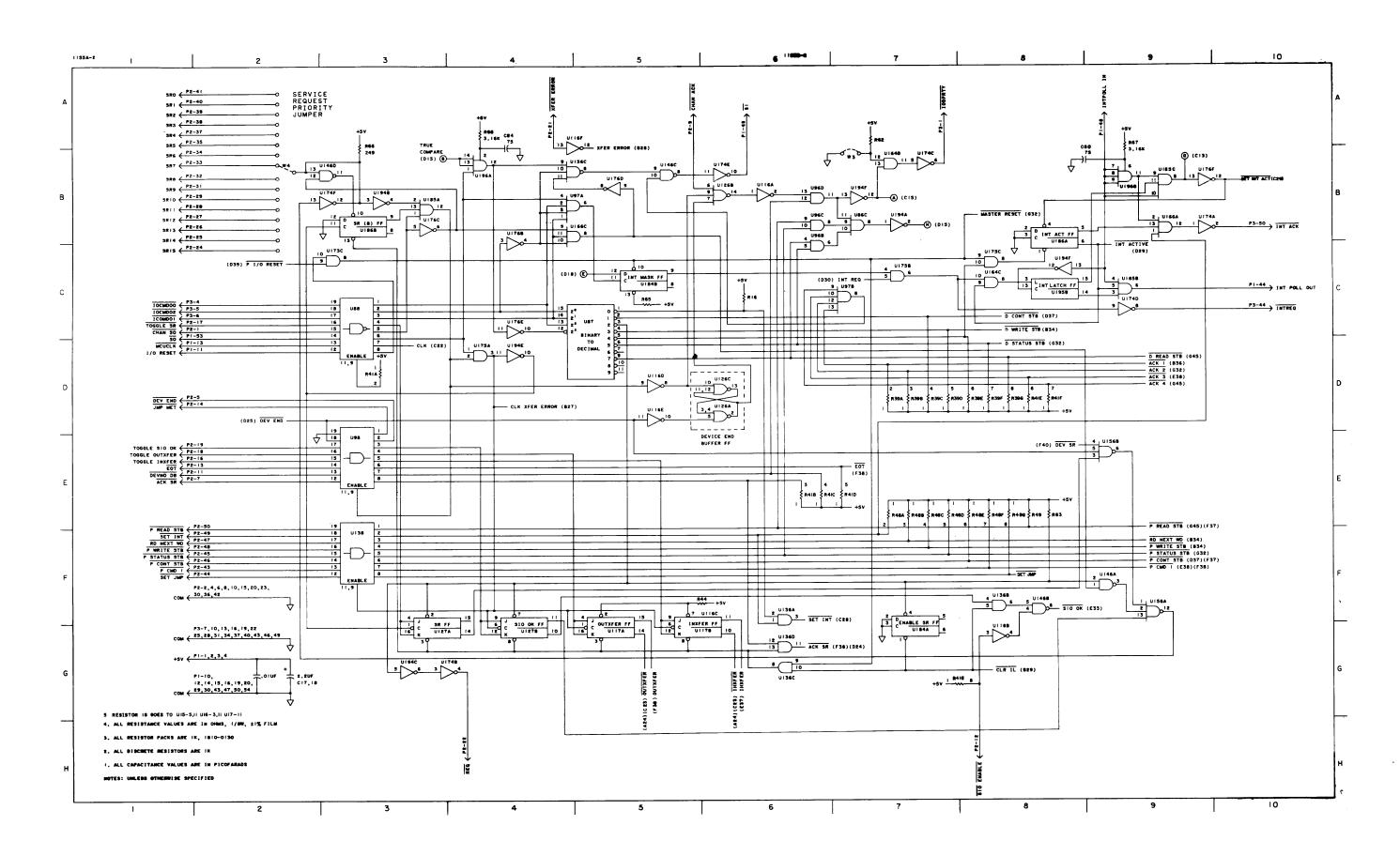


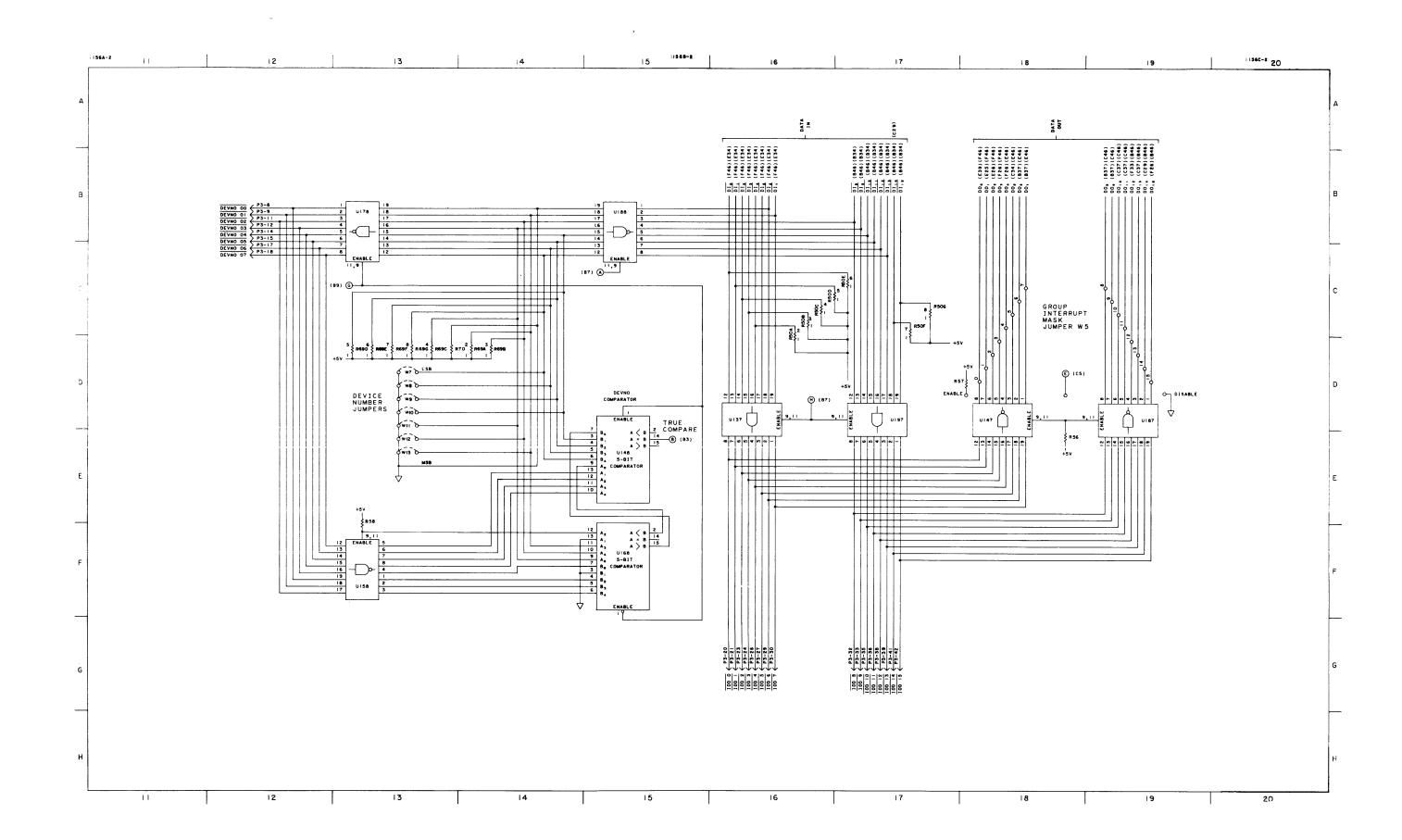
Diagnostic Hardware Assembly, 30049-60003, Sheet 1 of 3

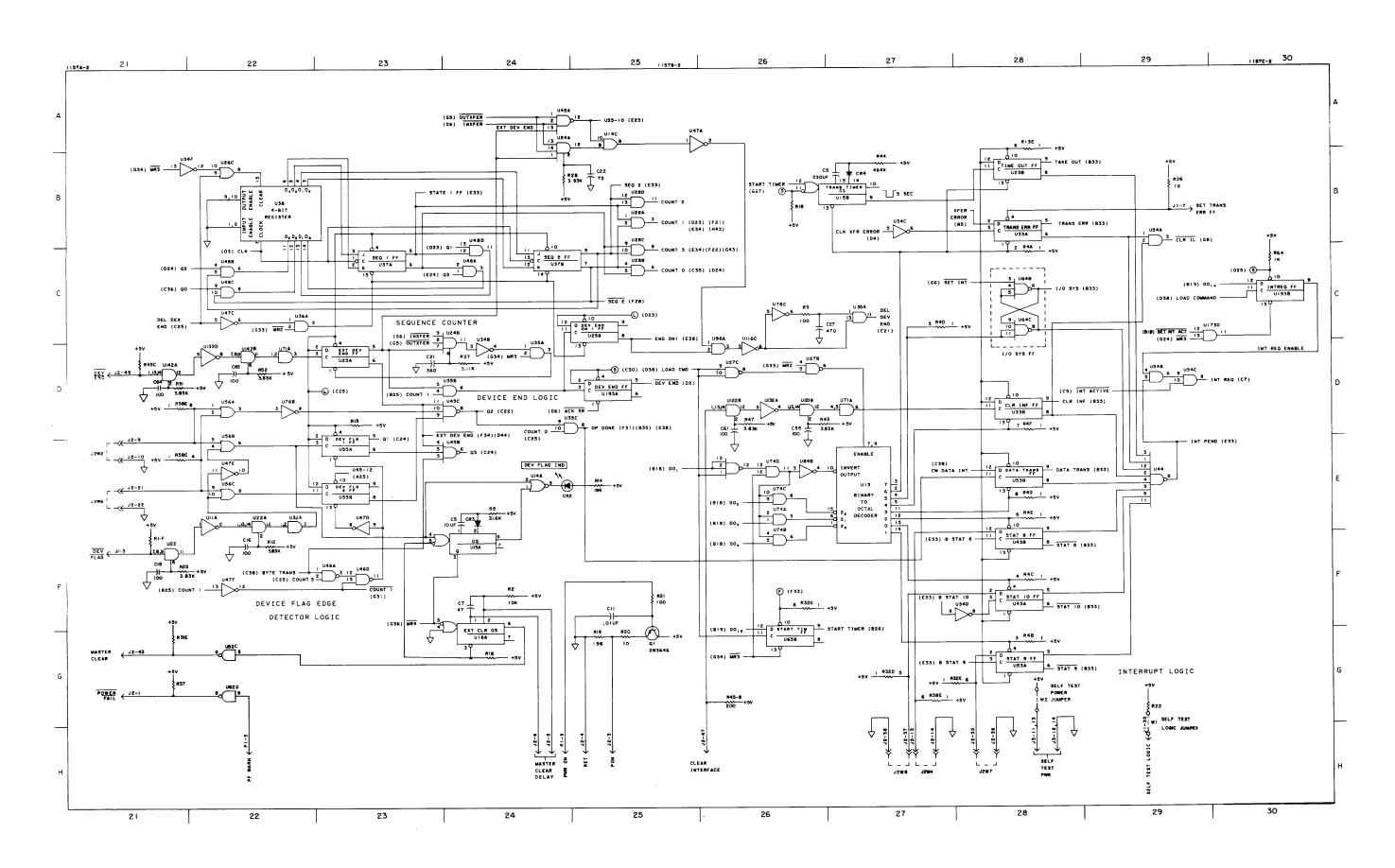


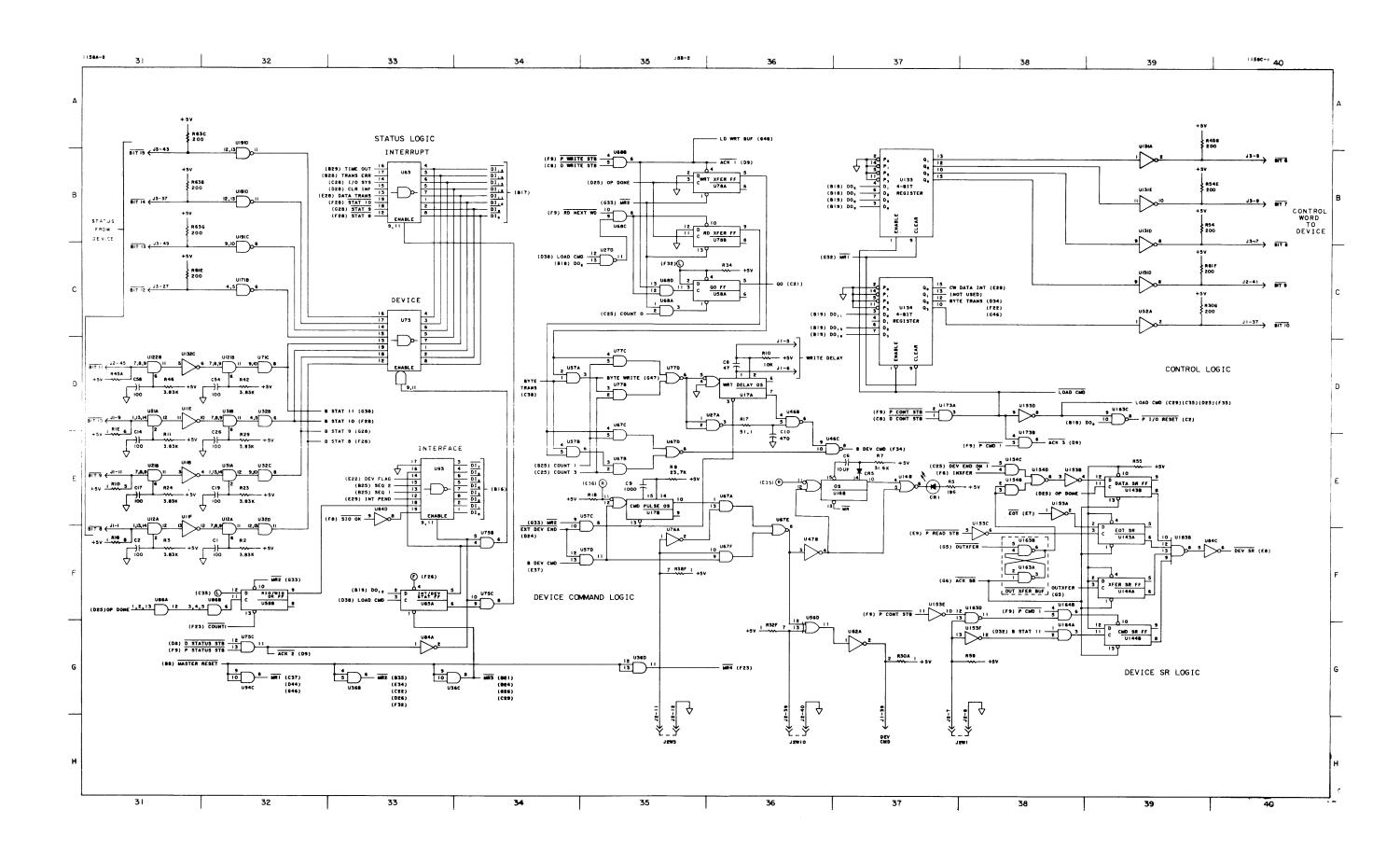


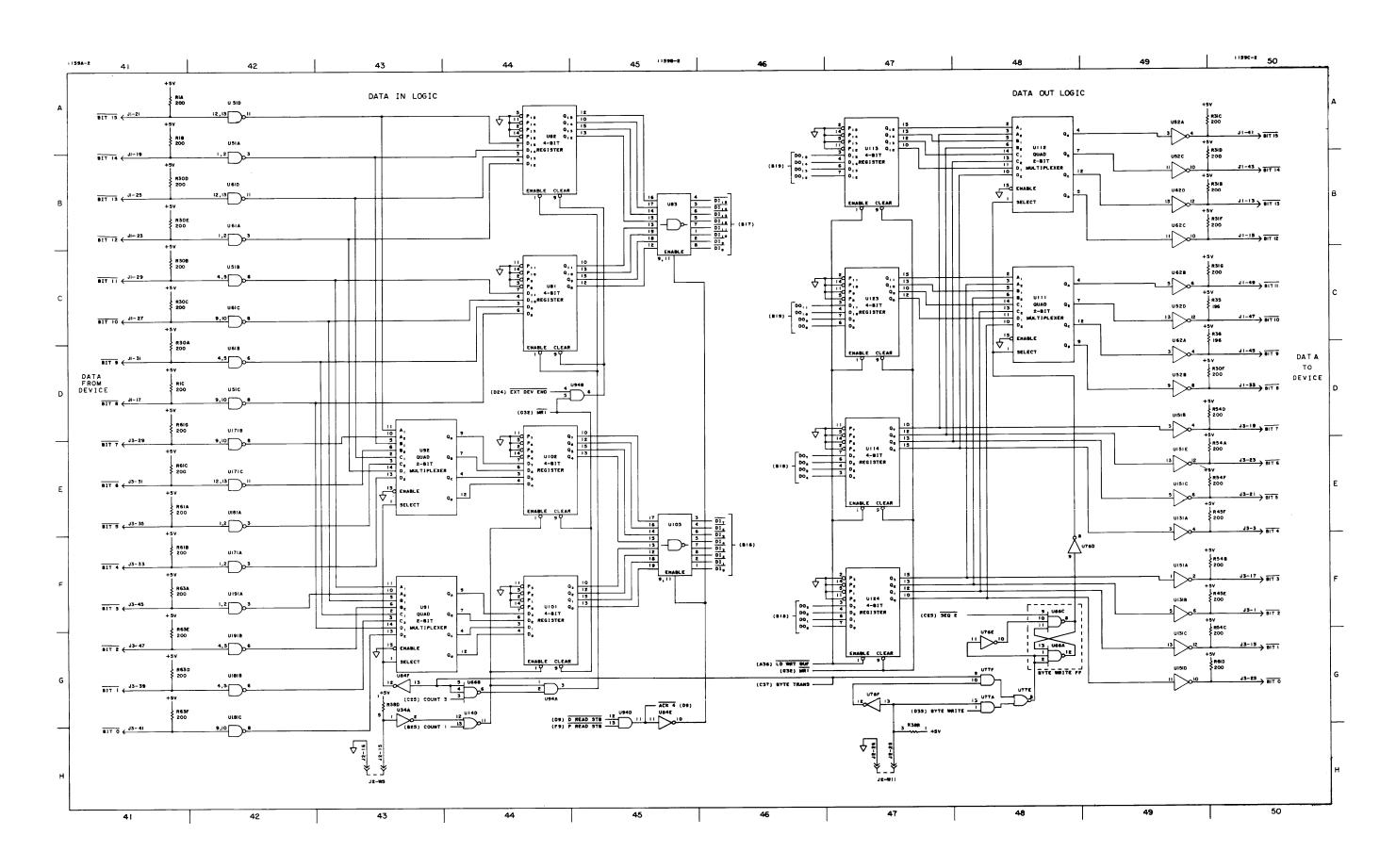


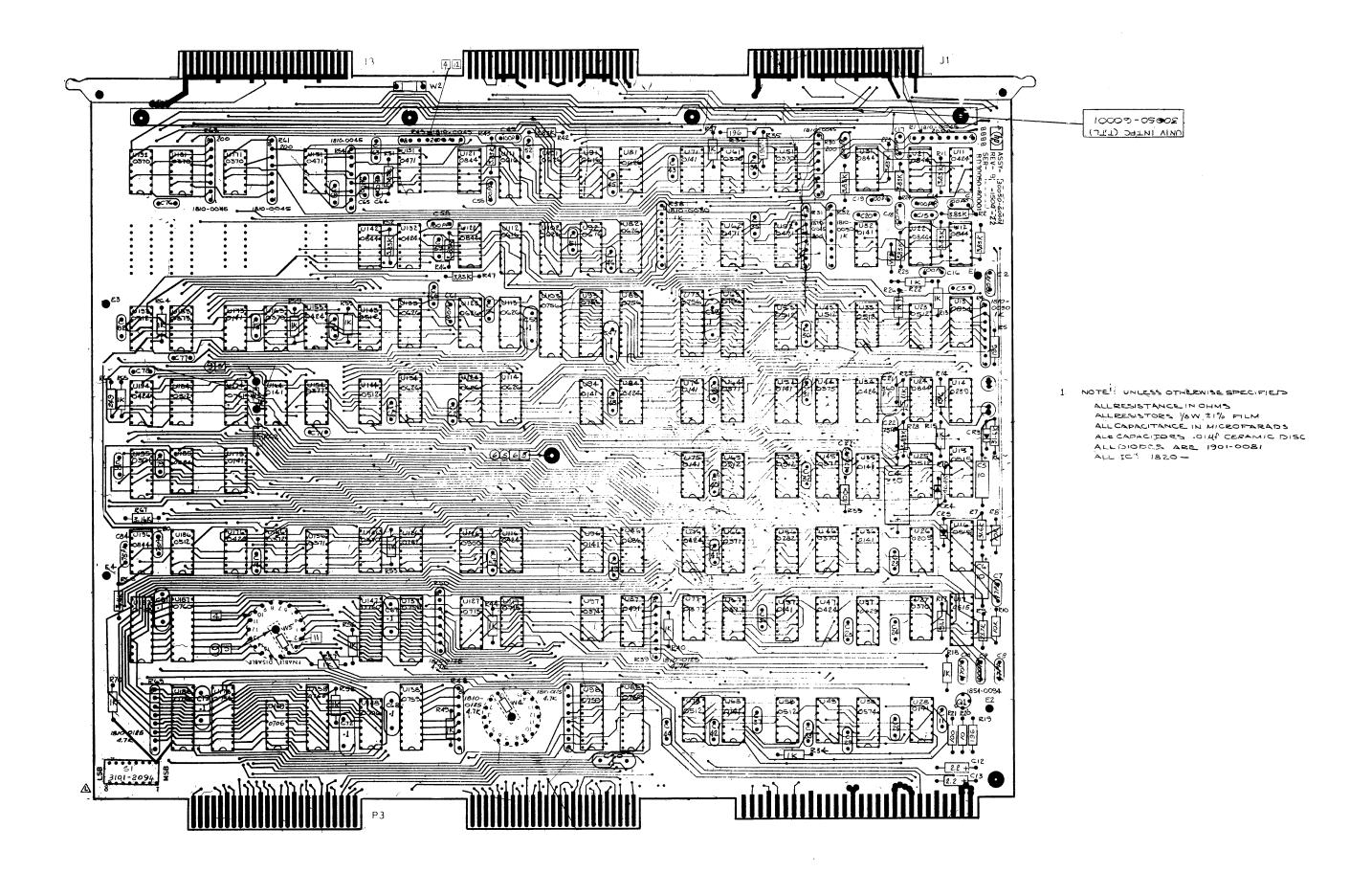


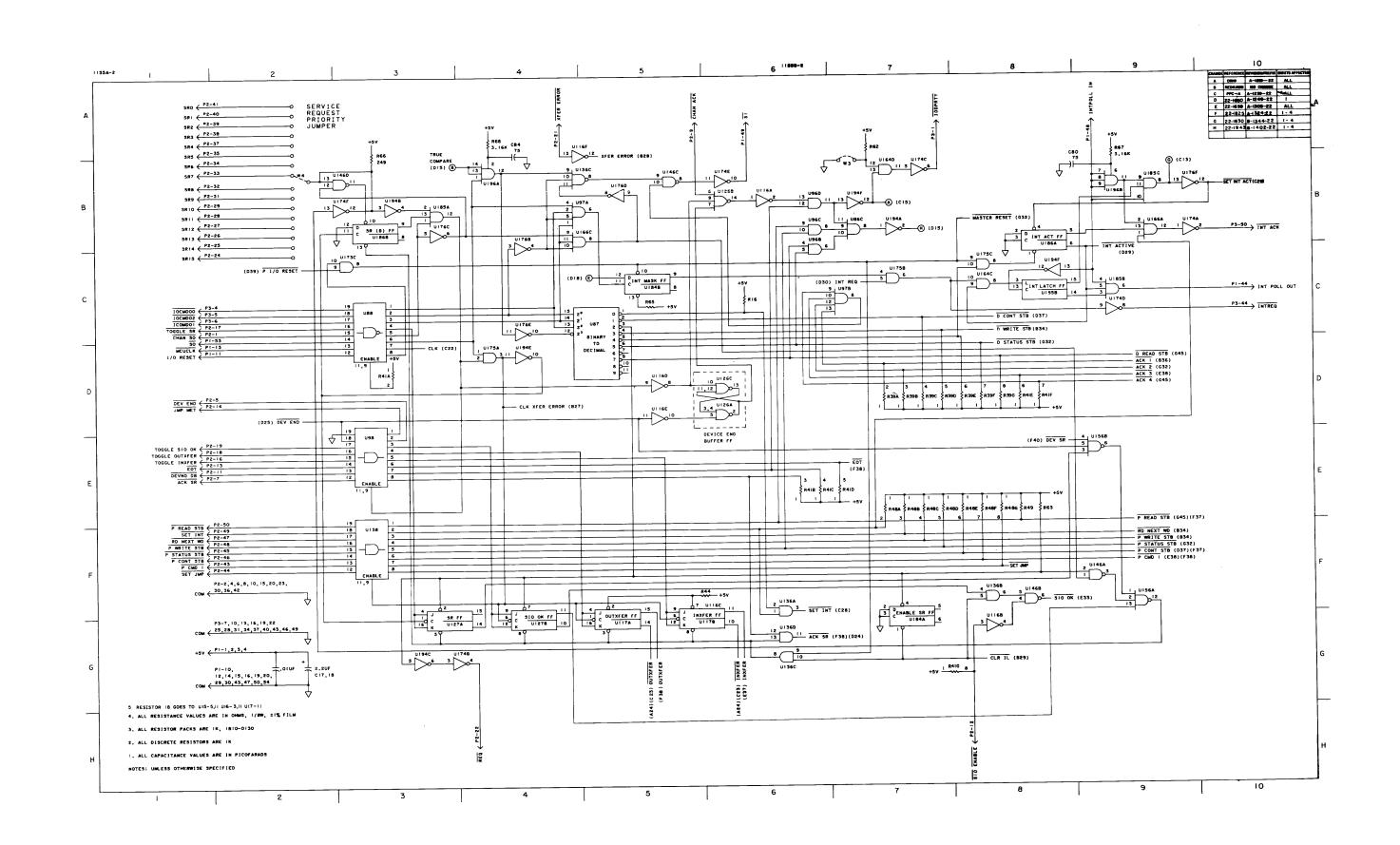


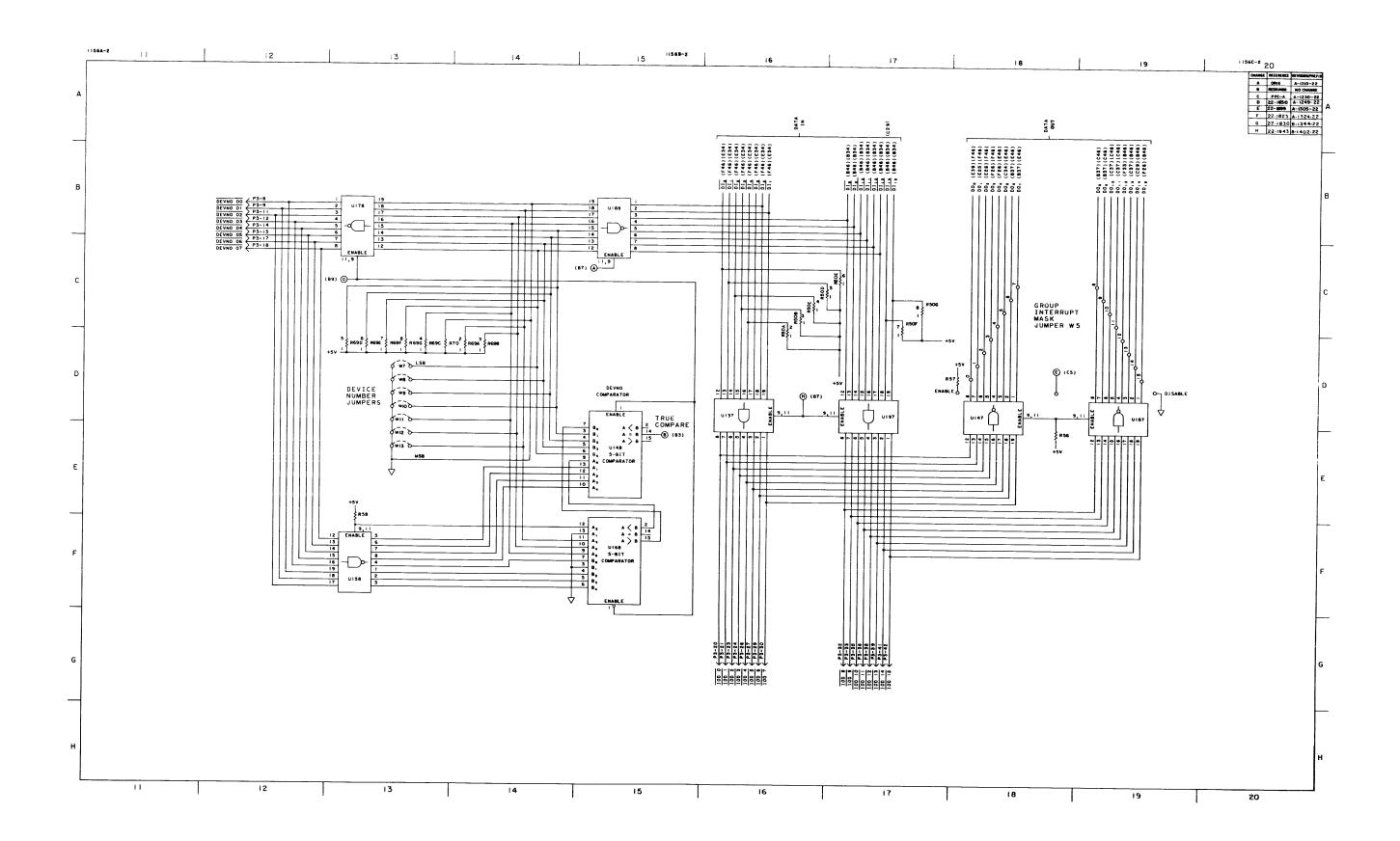


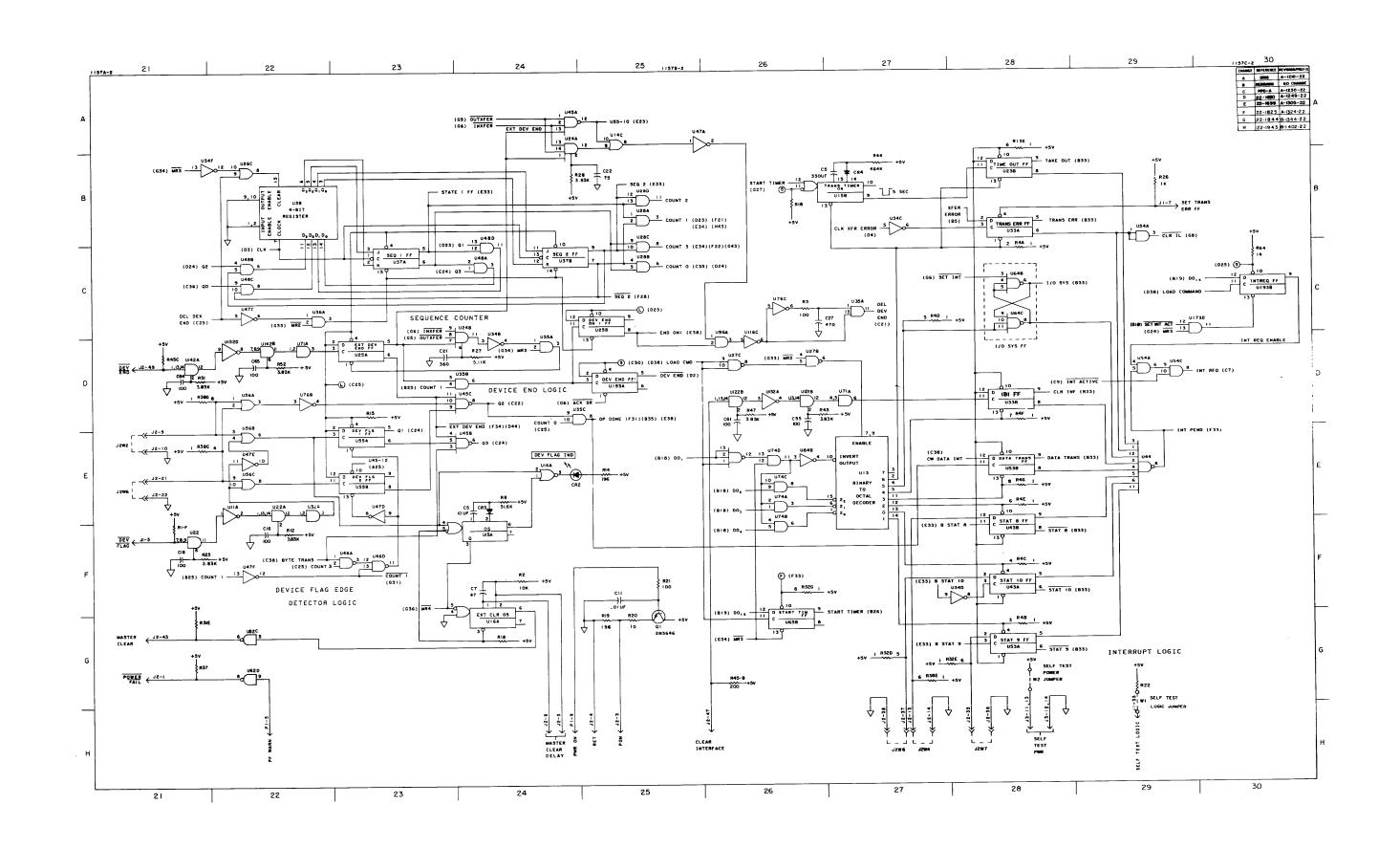


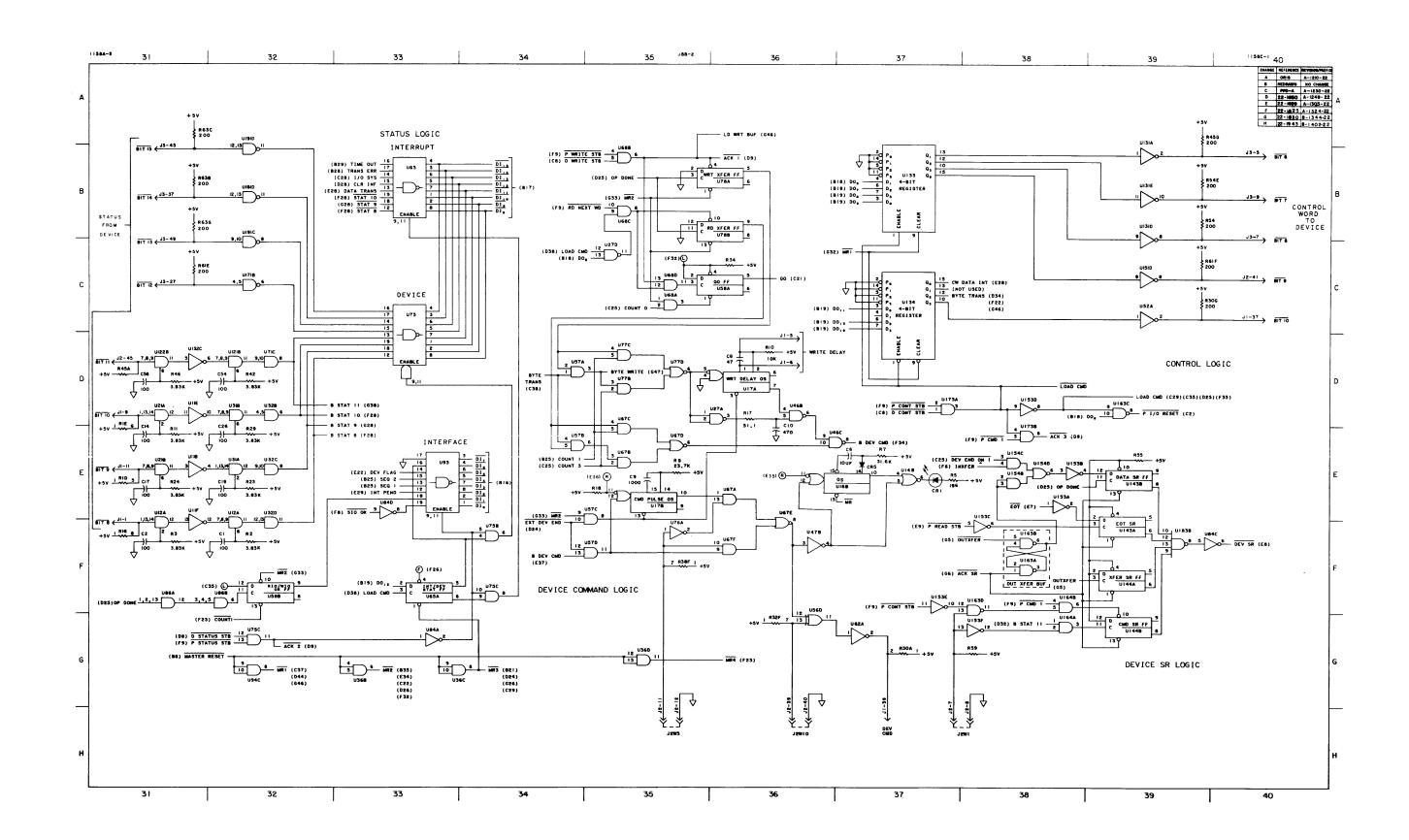


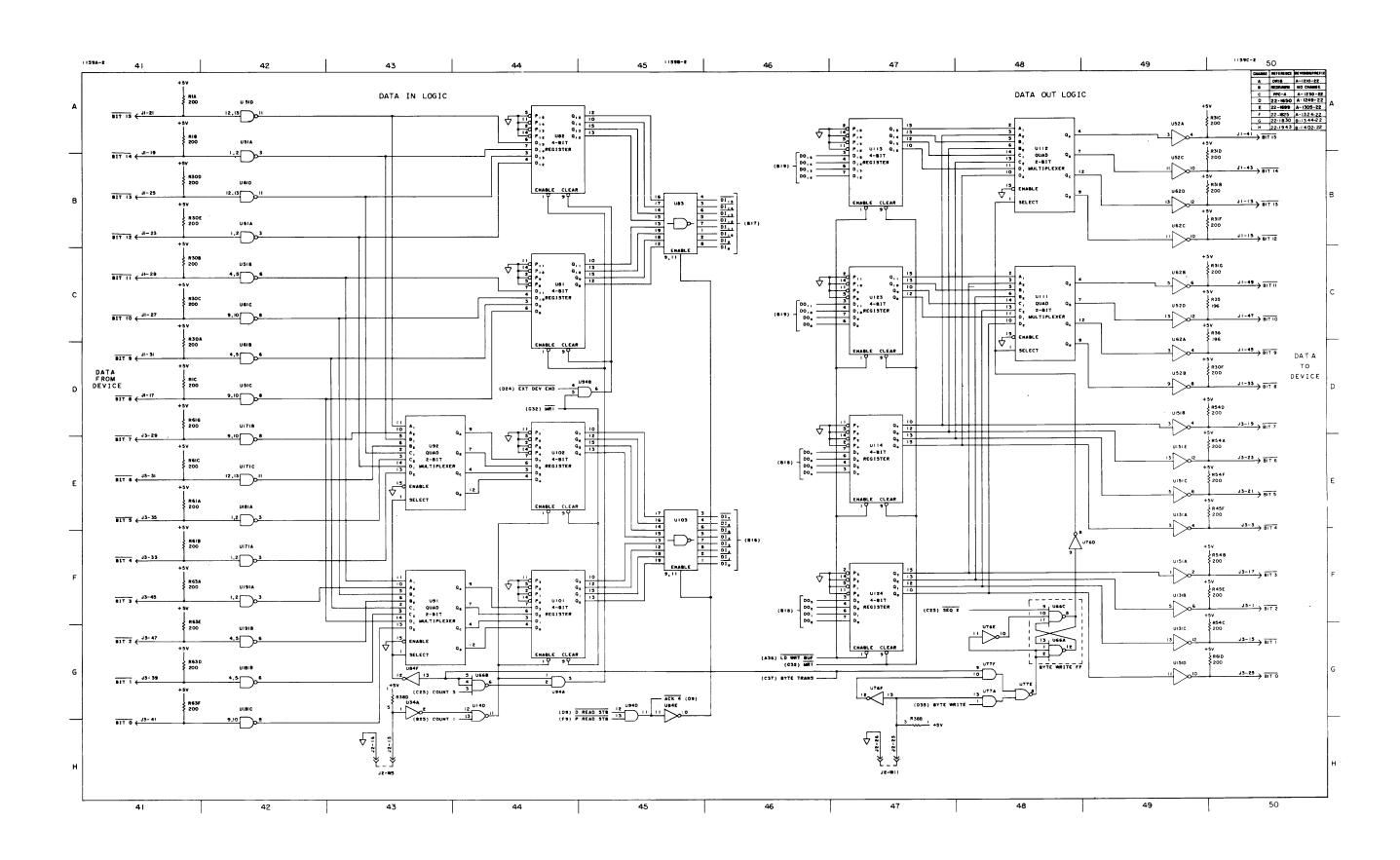


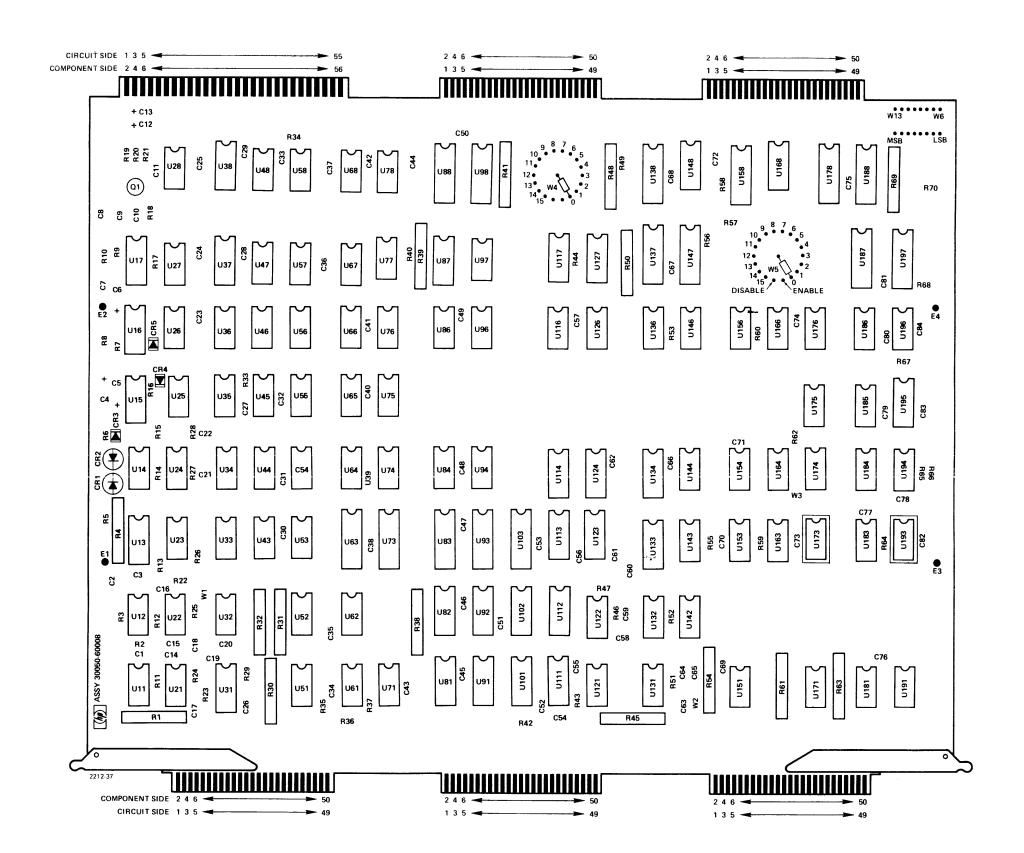


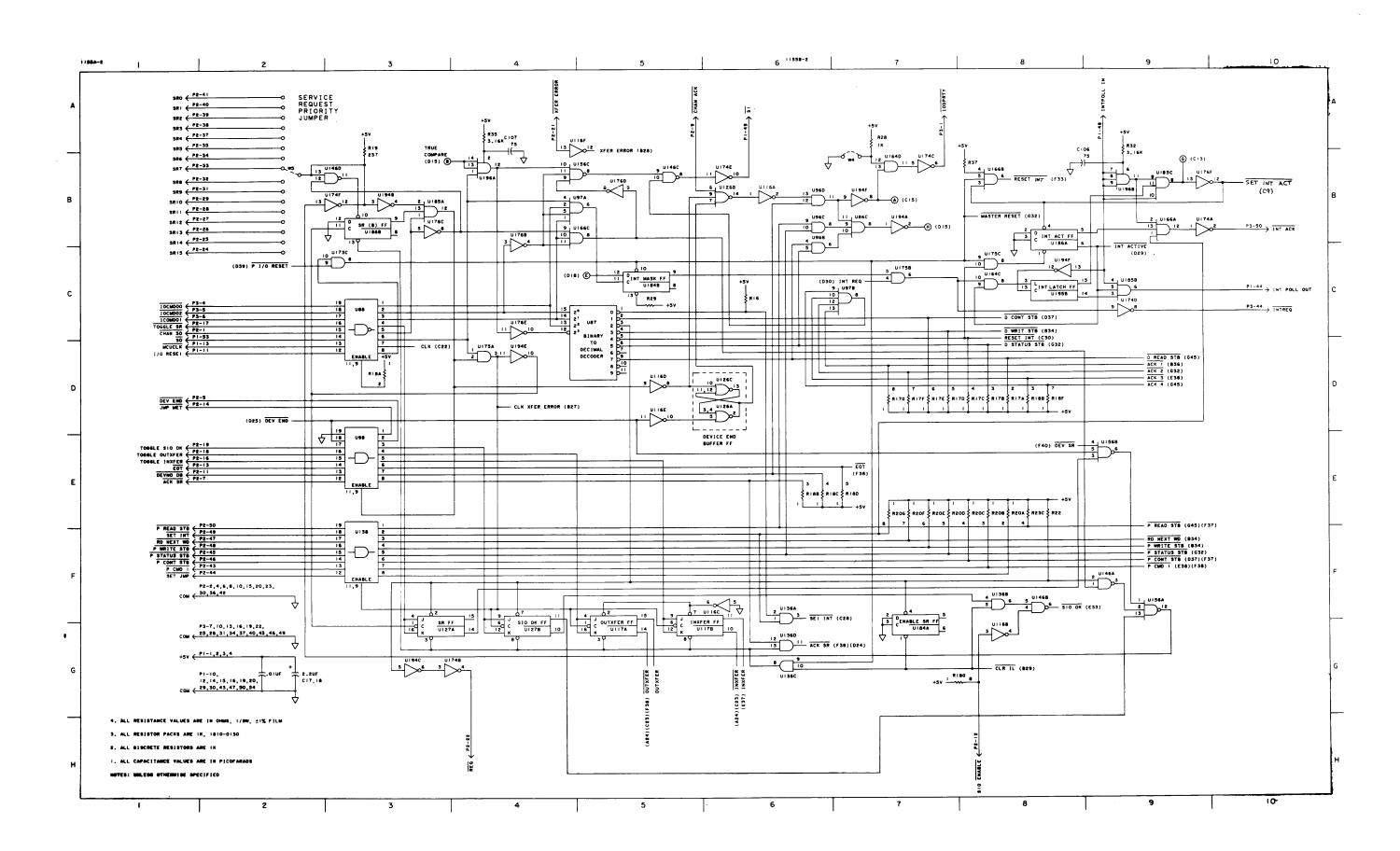


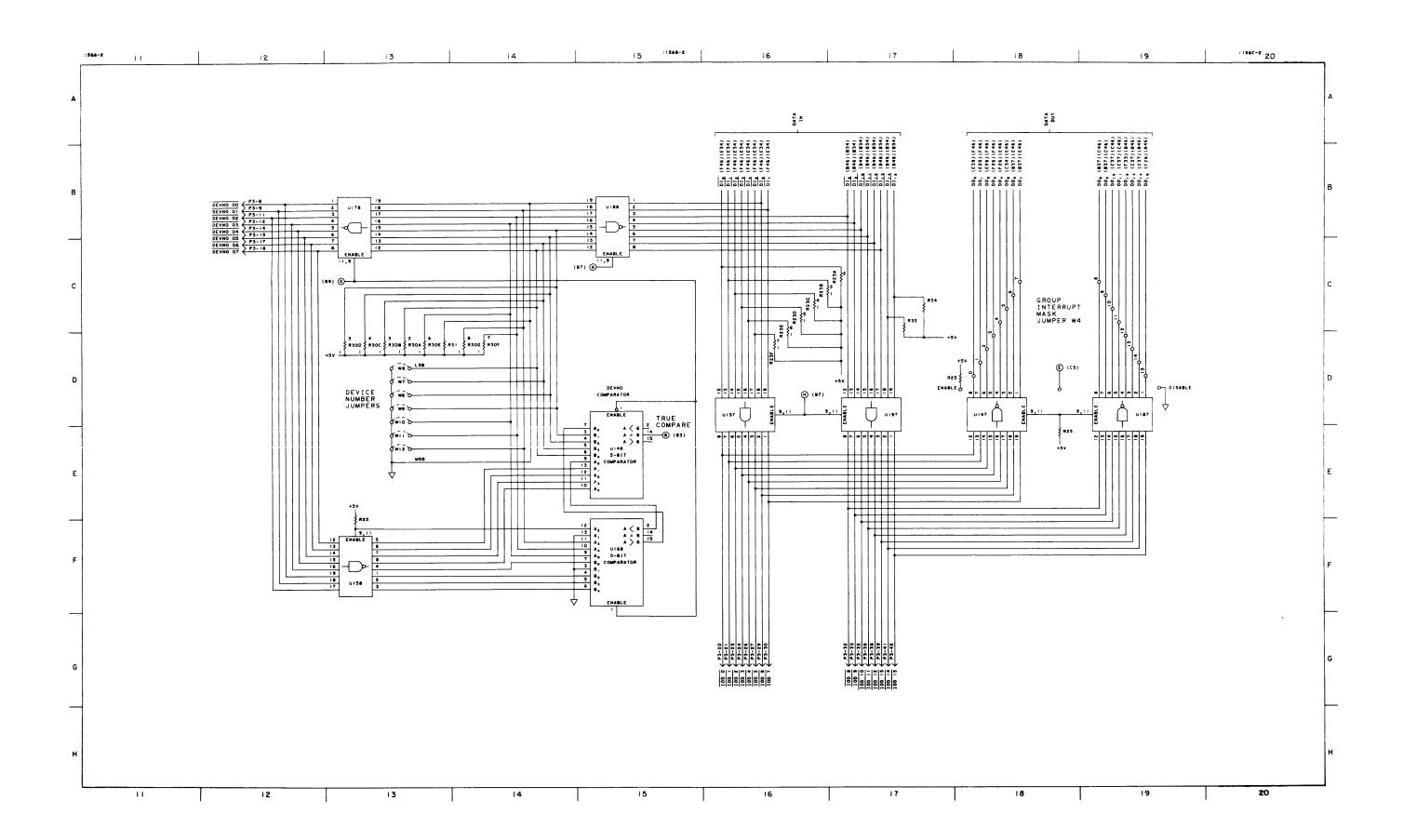


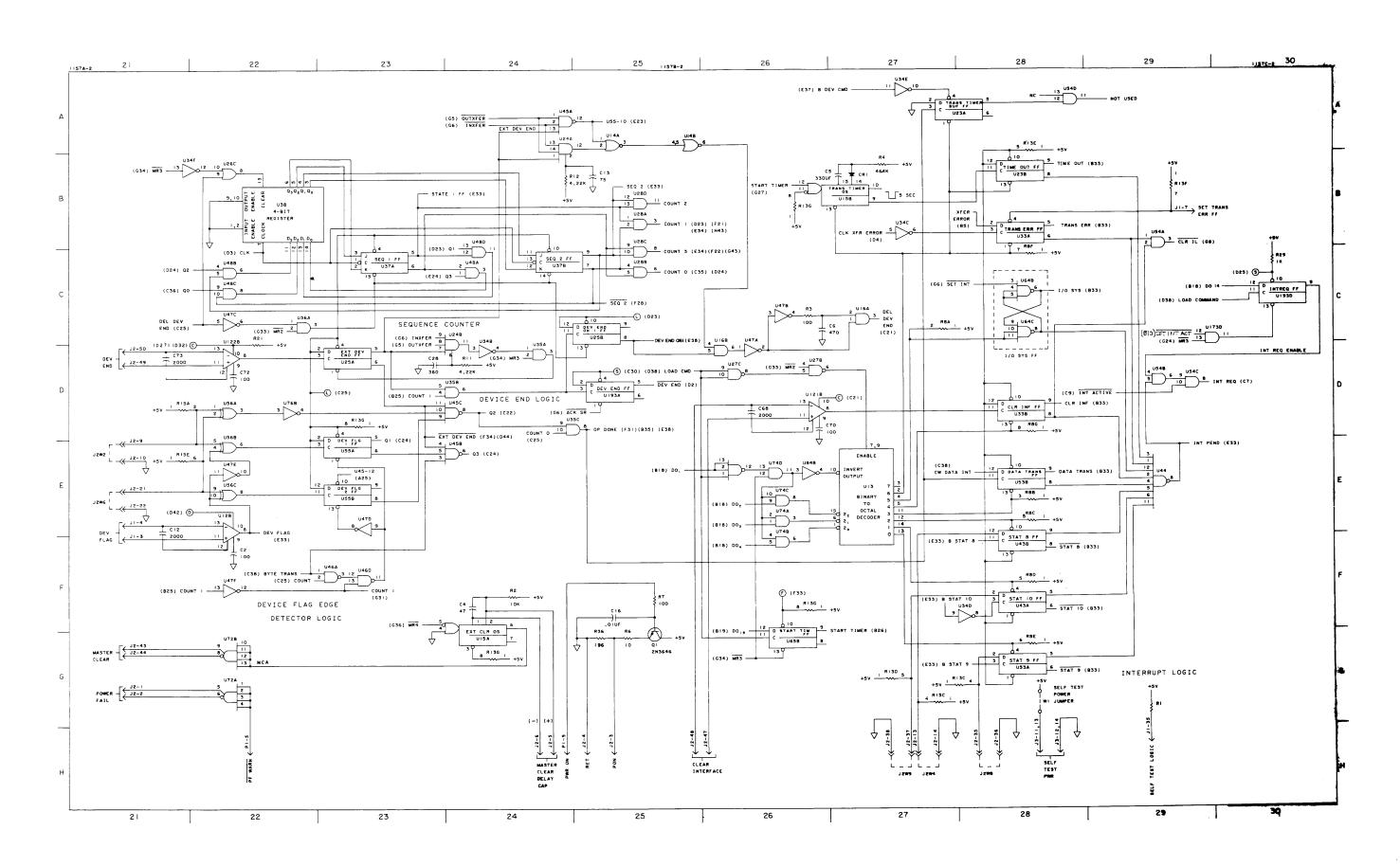


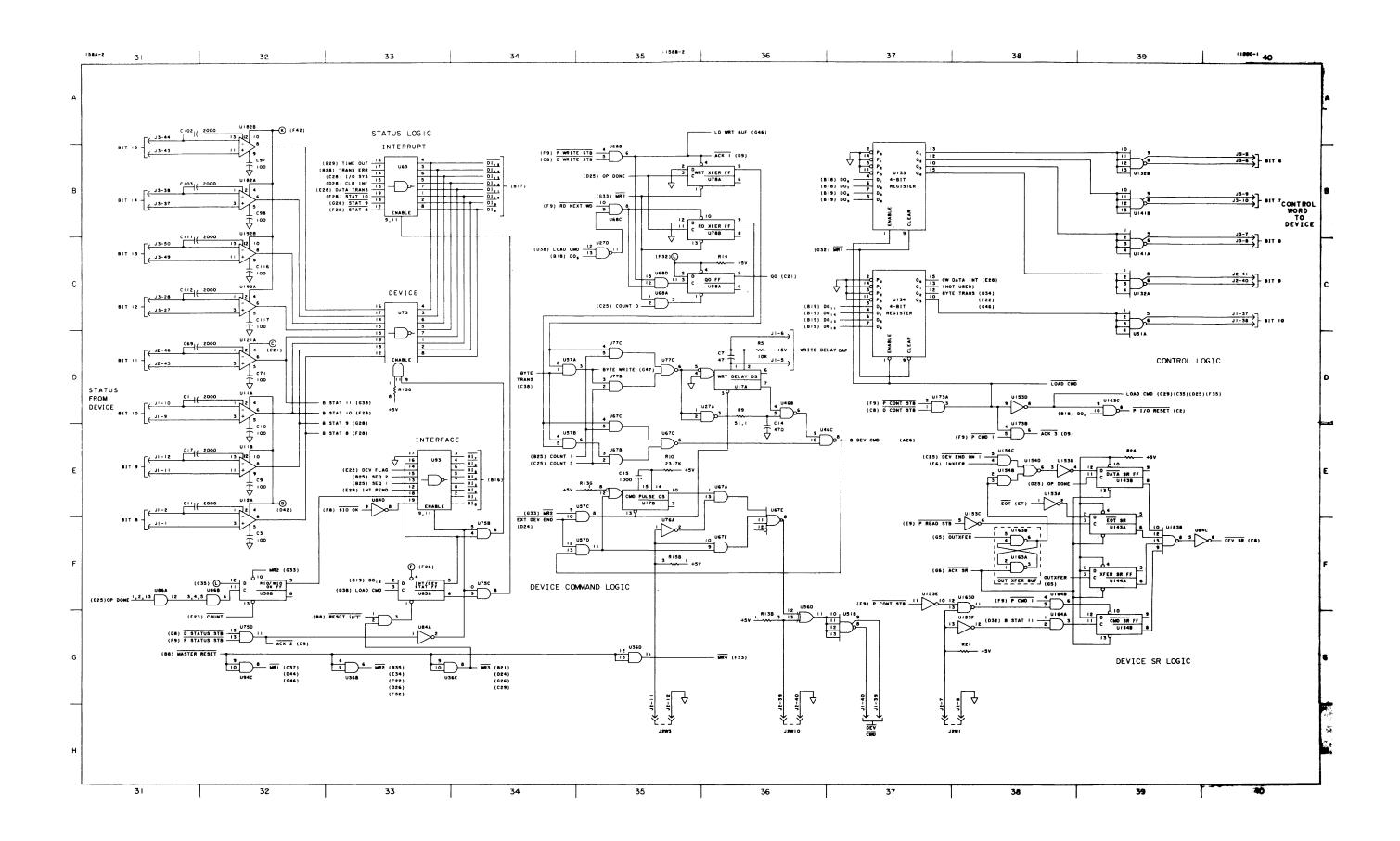


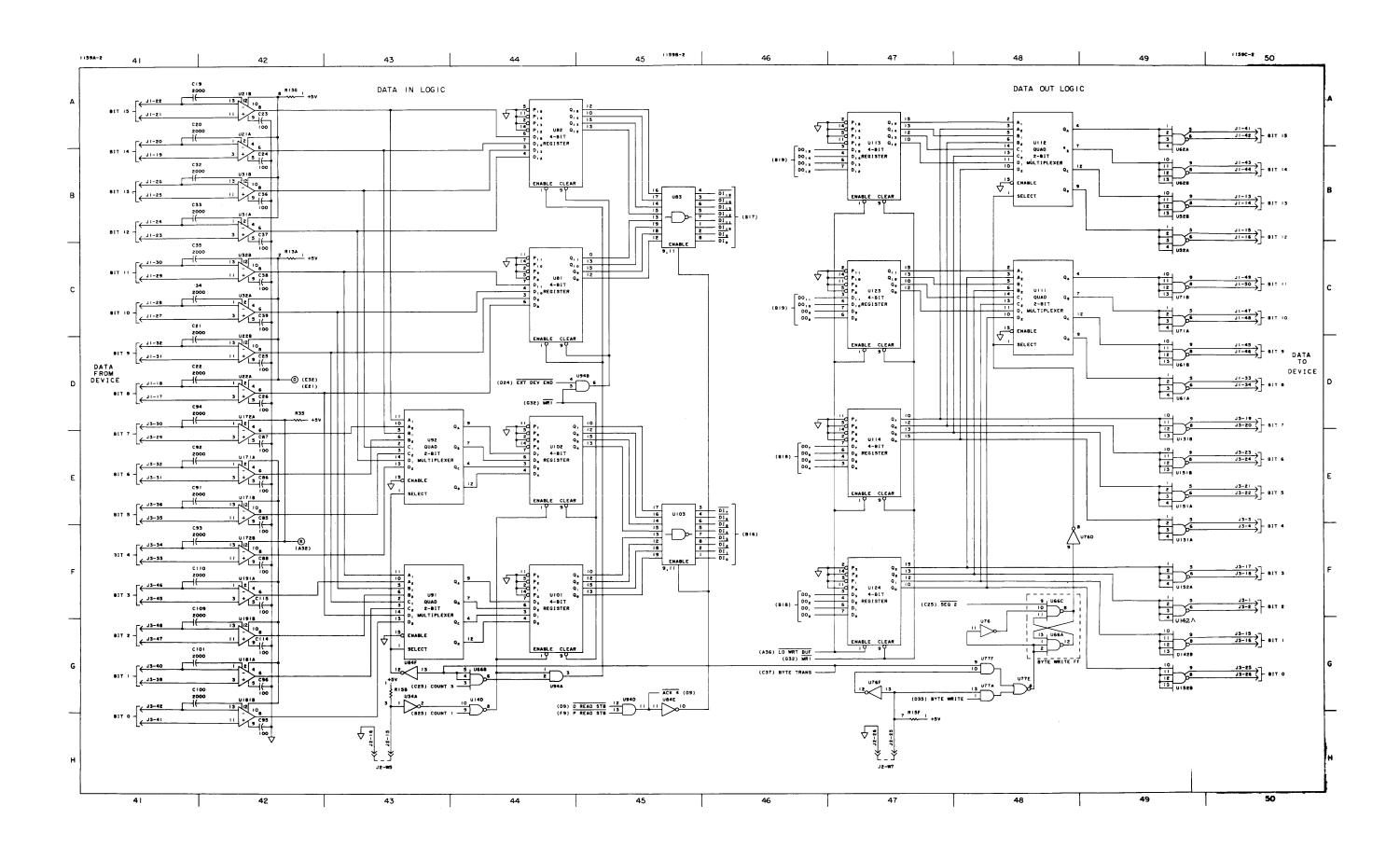


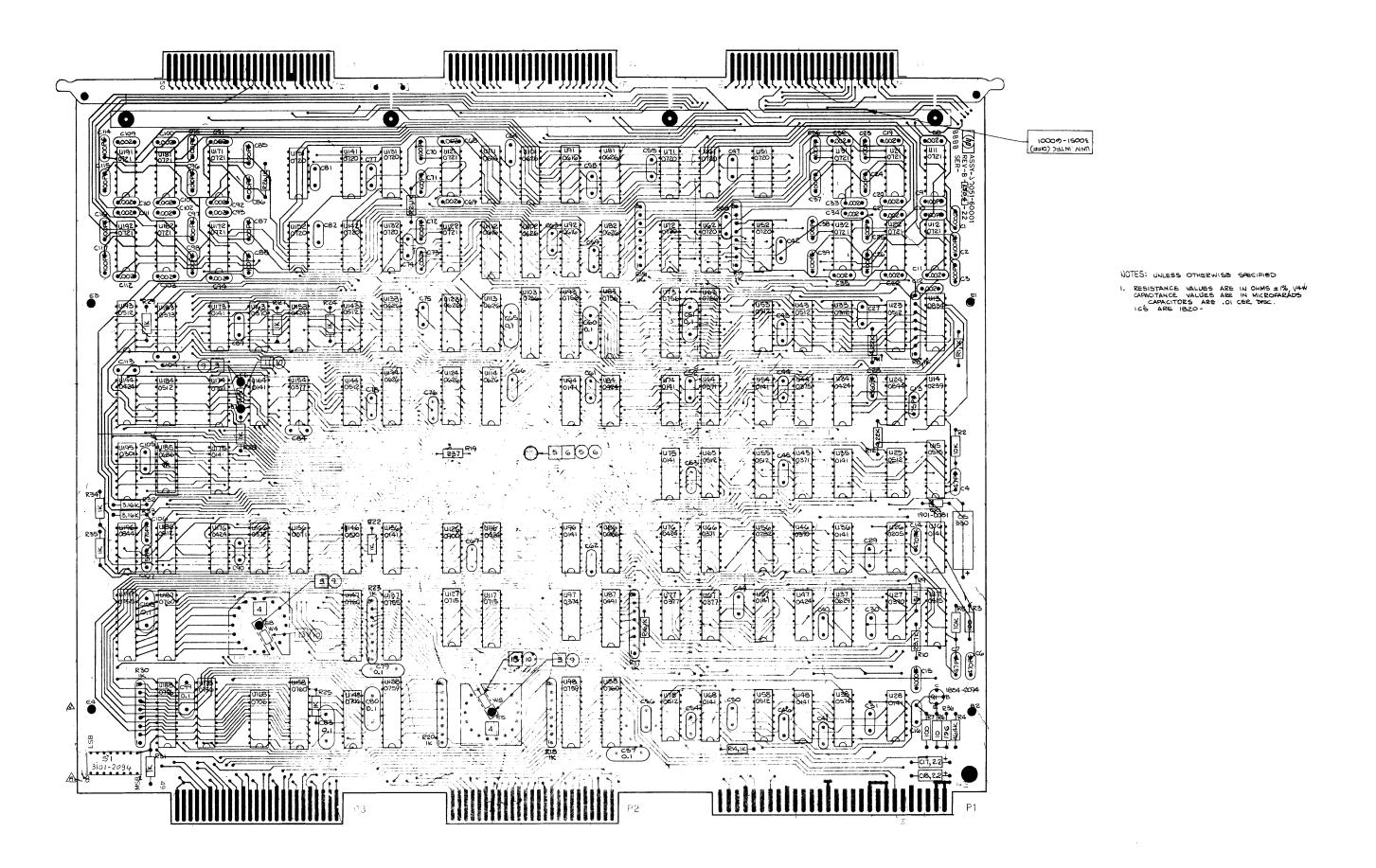


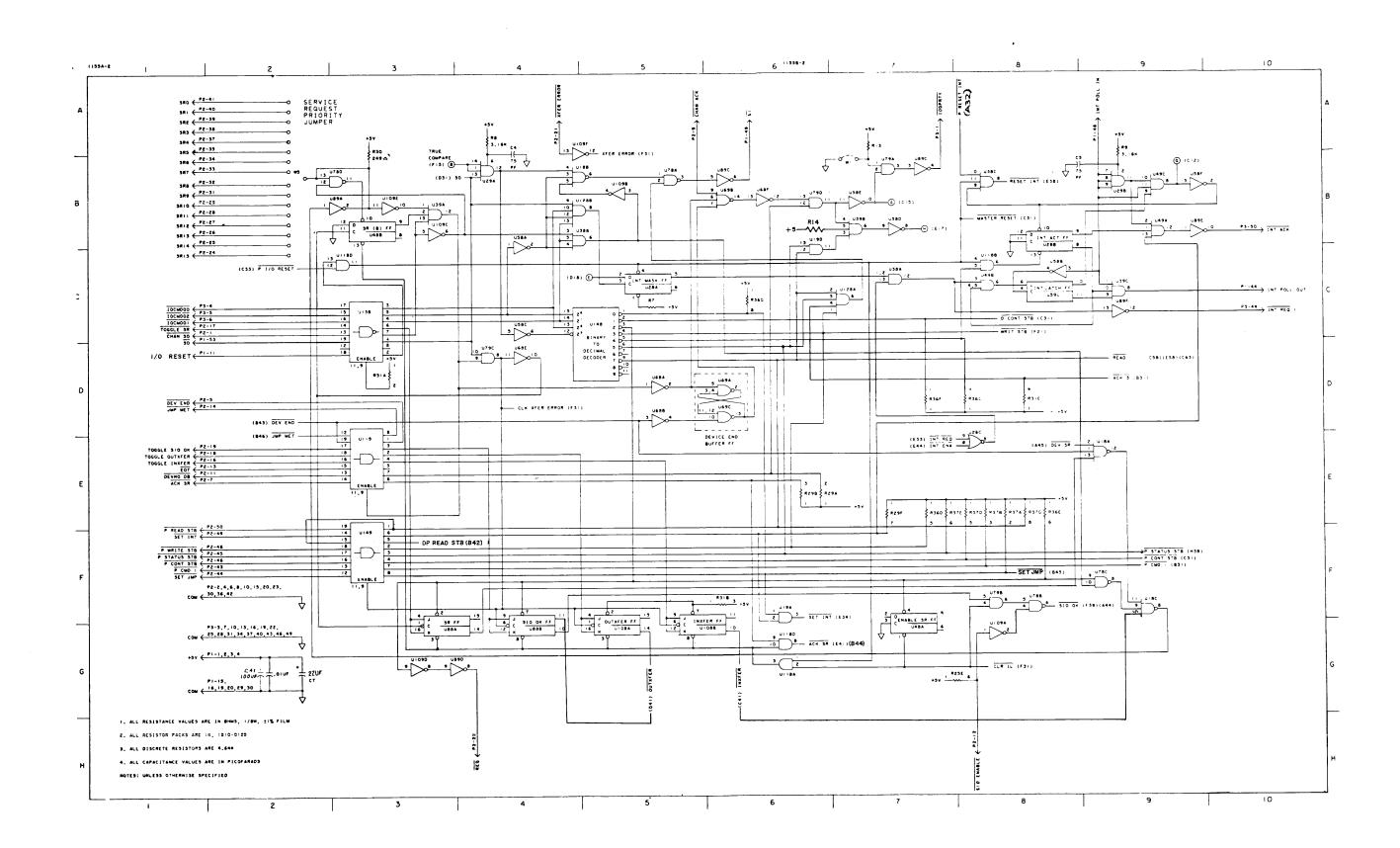


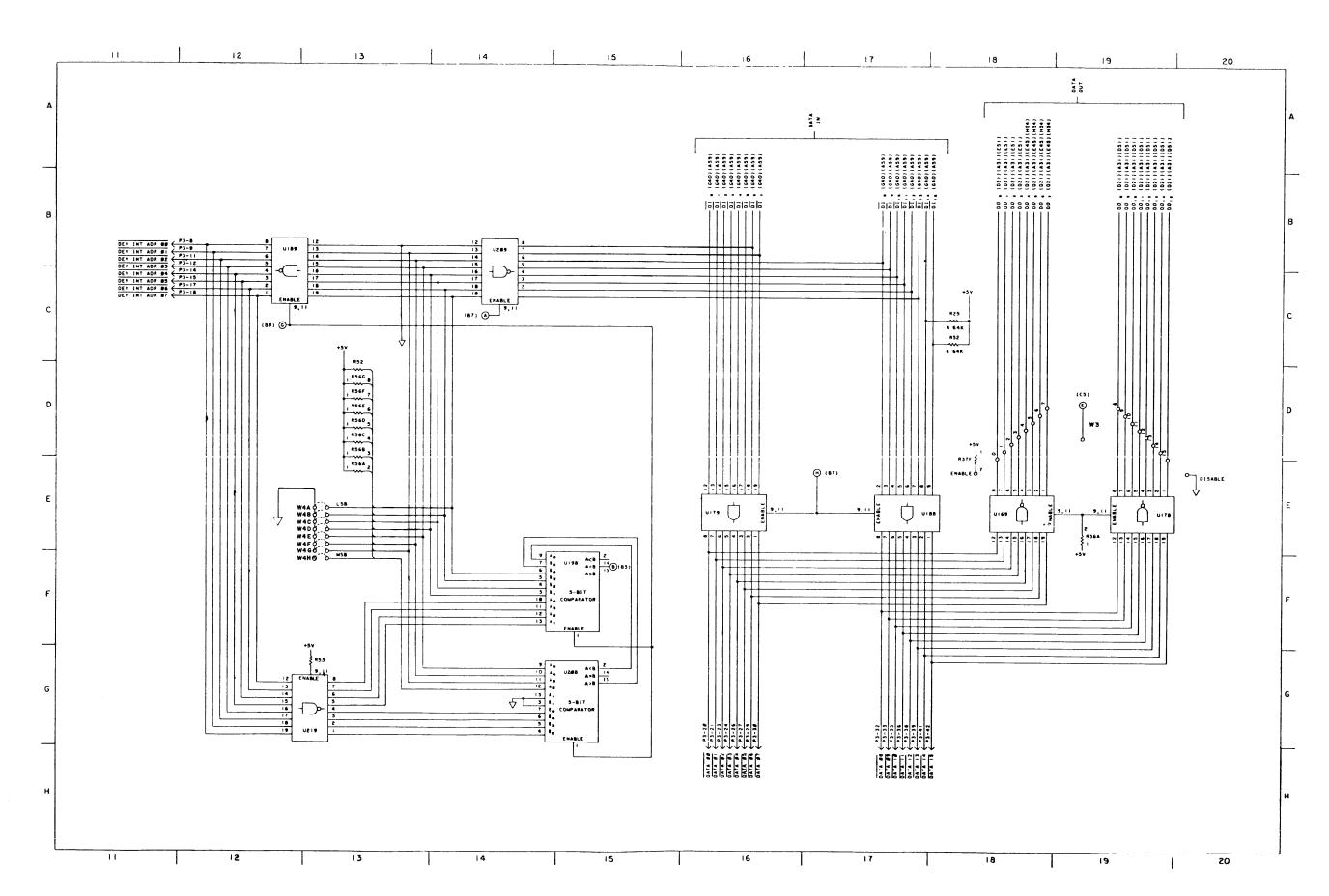


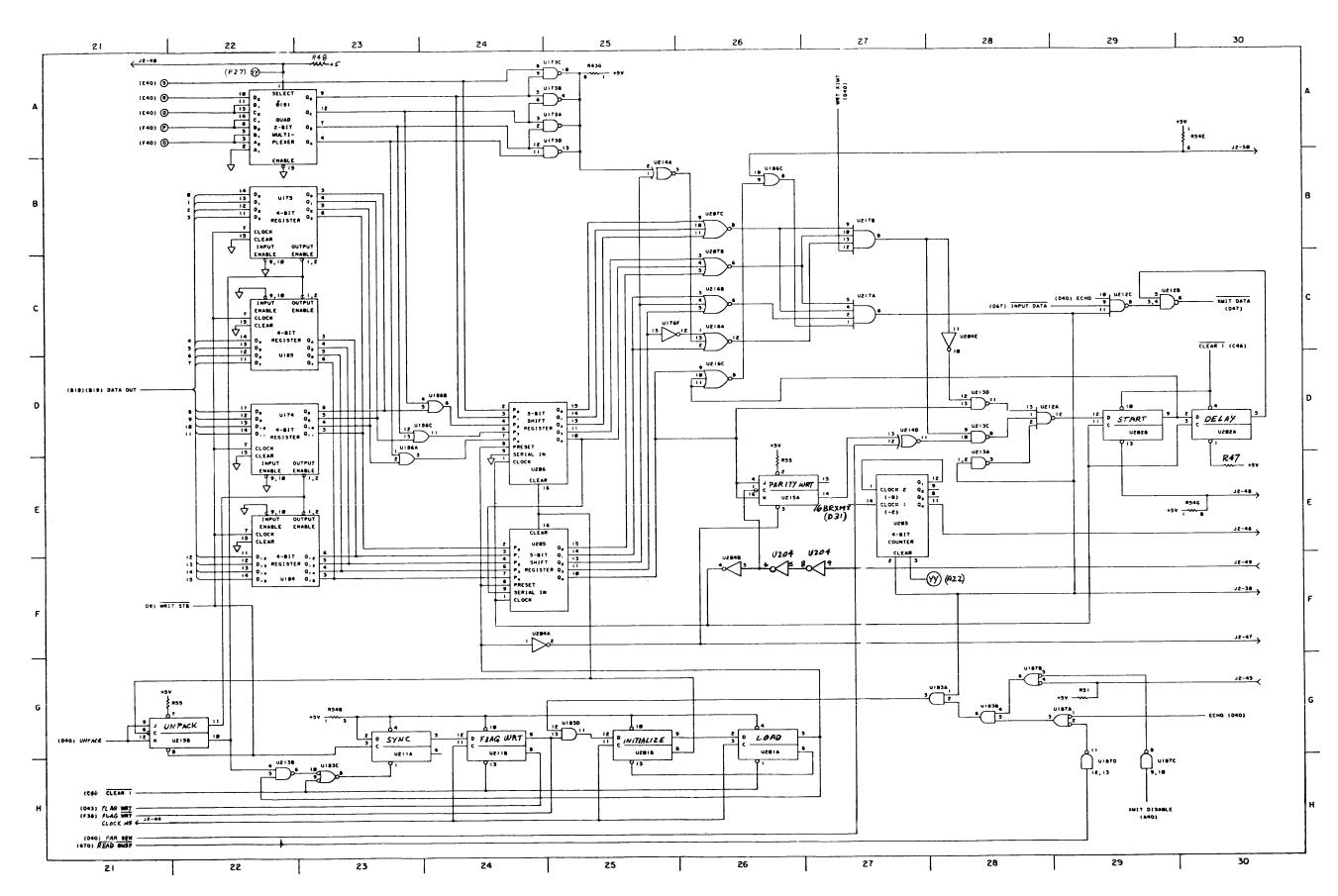


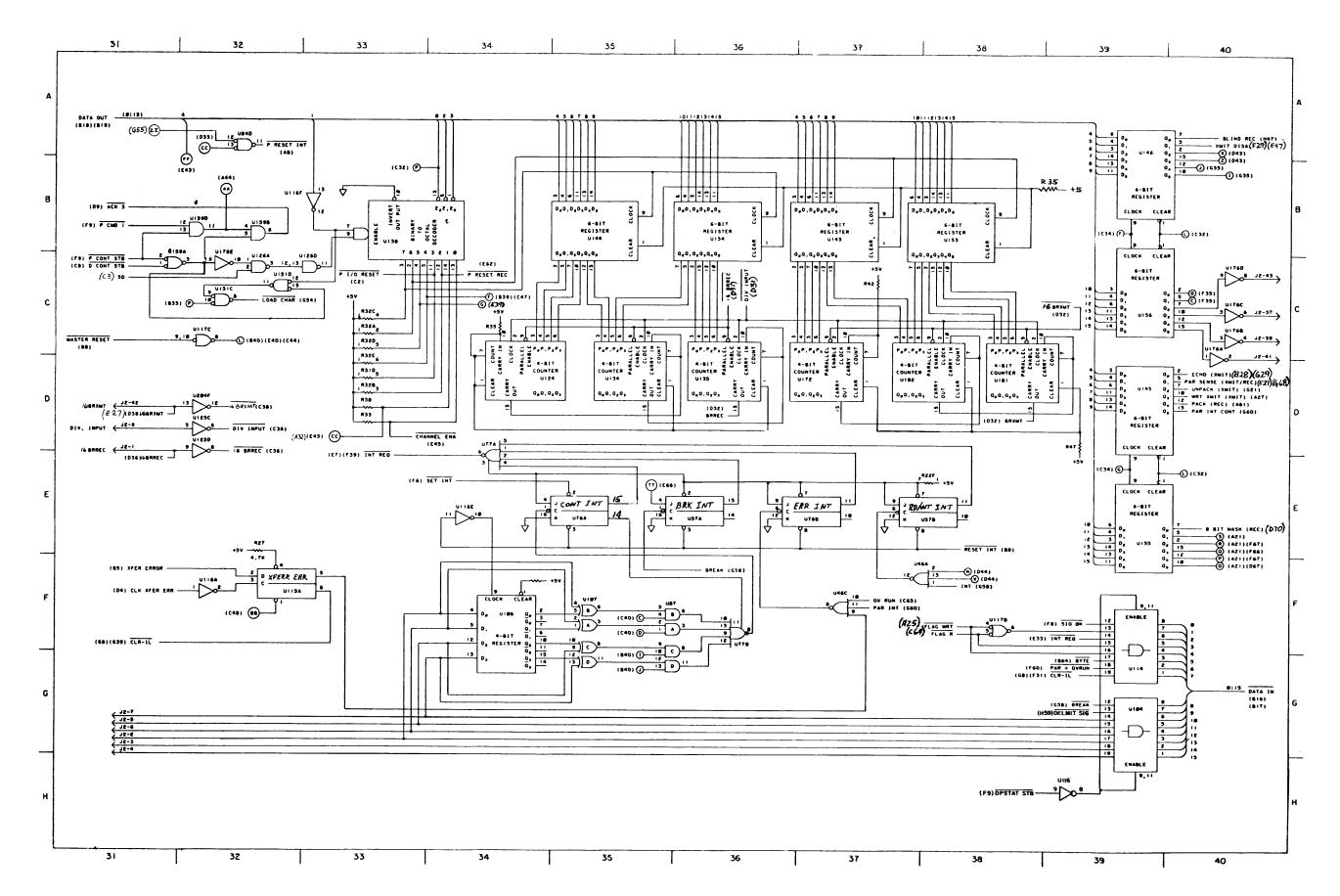


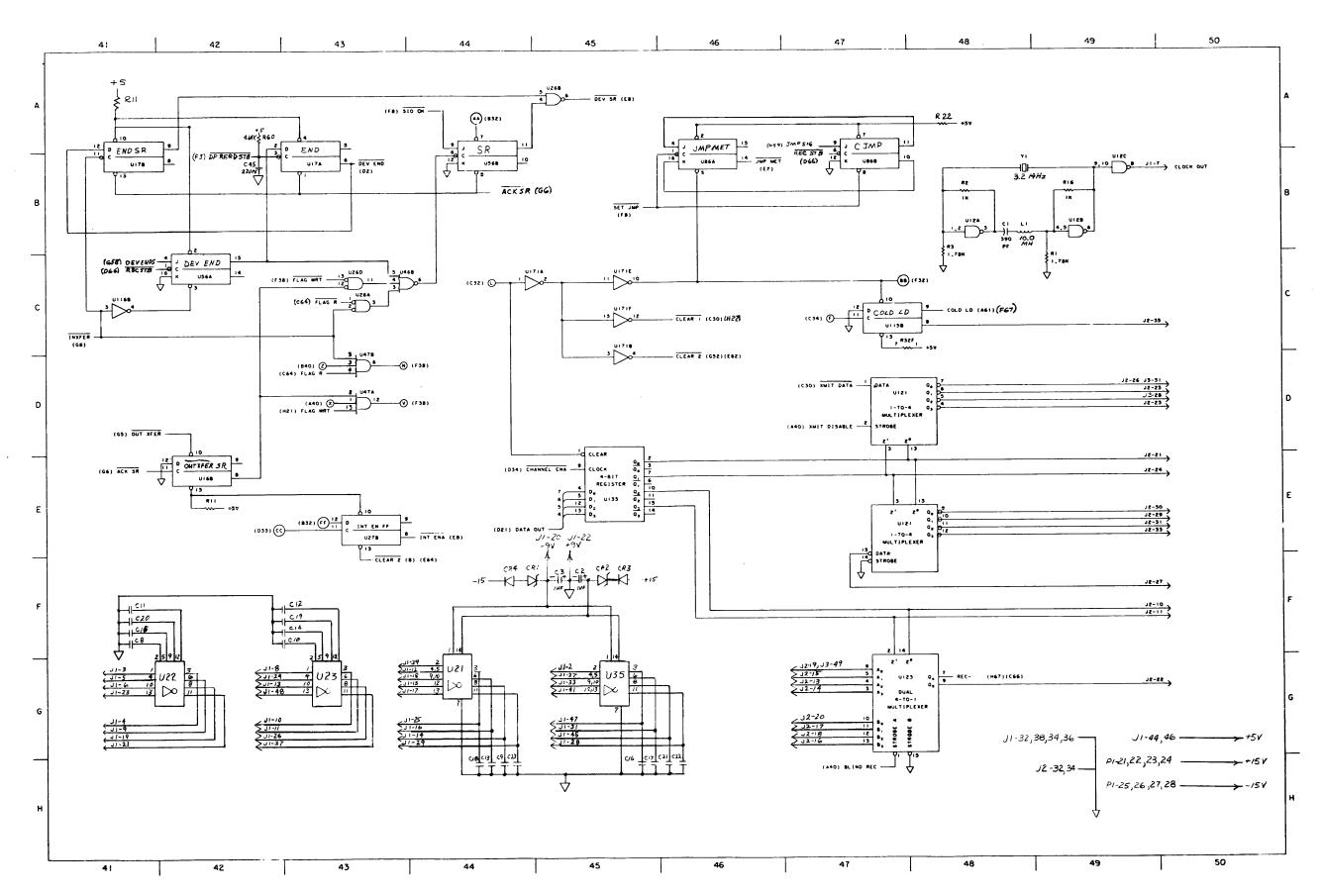


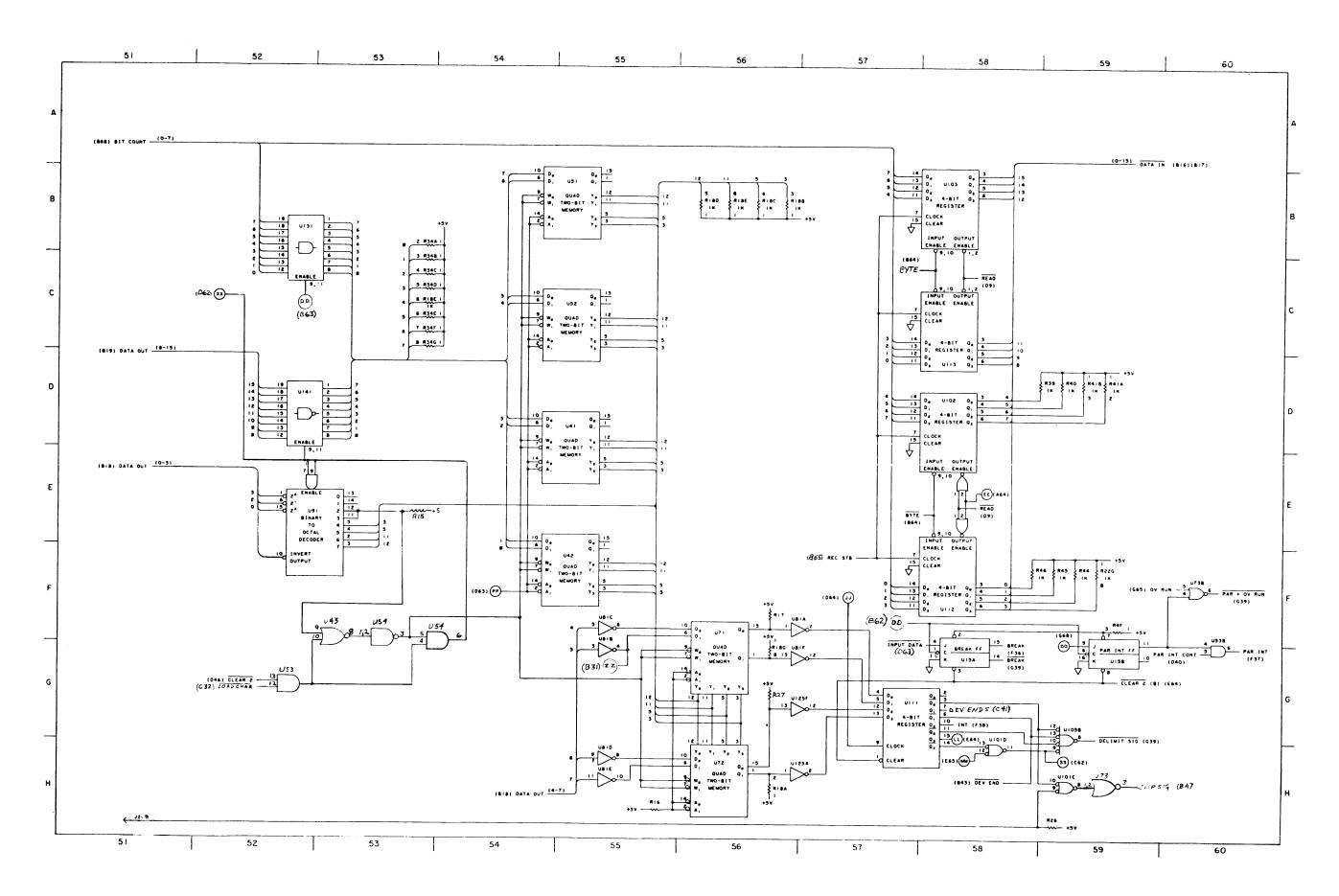


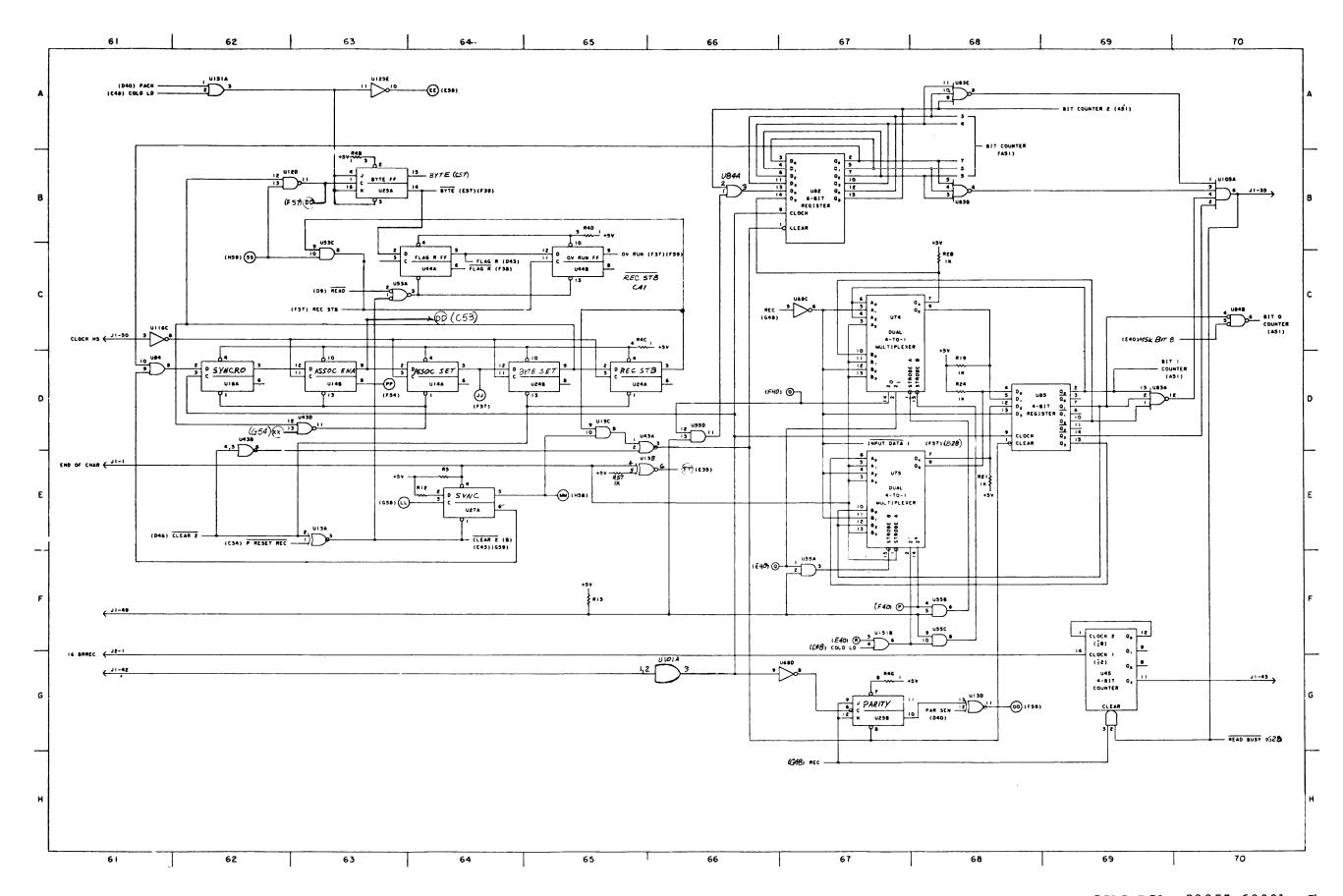


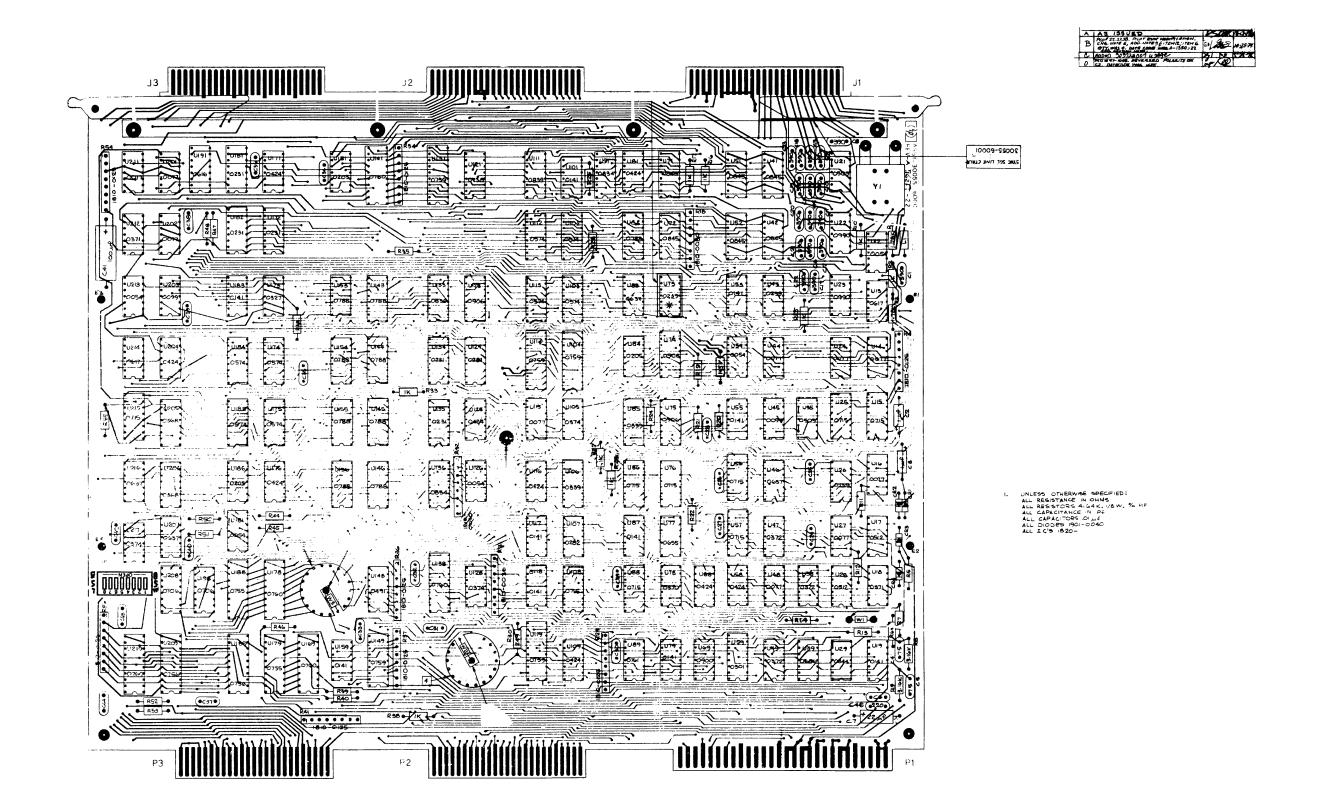


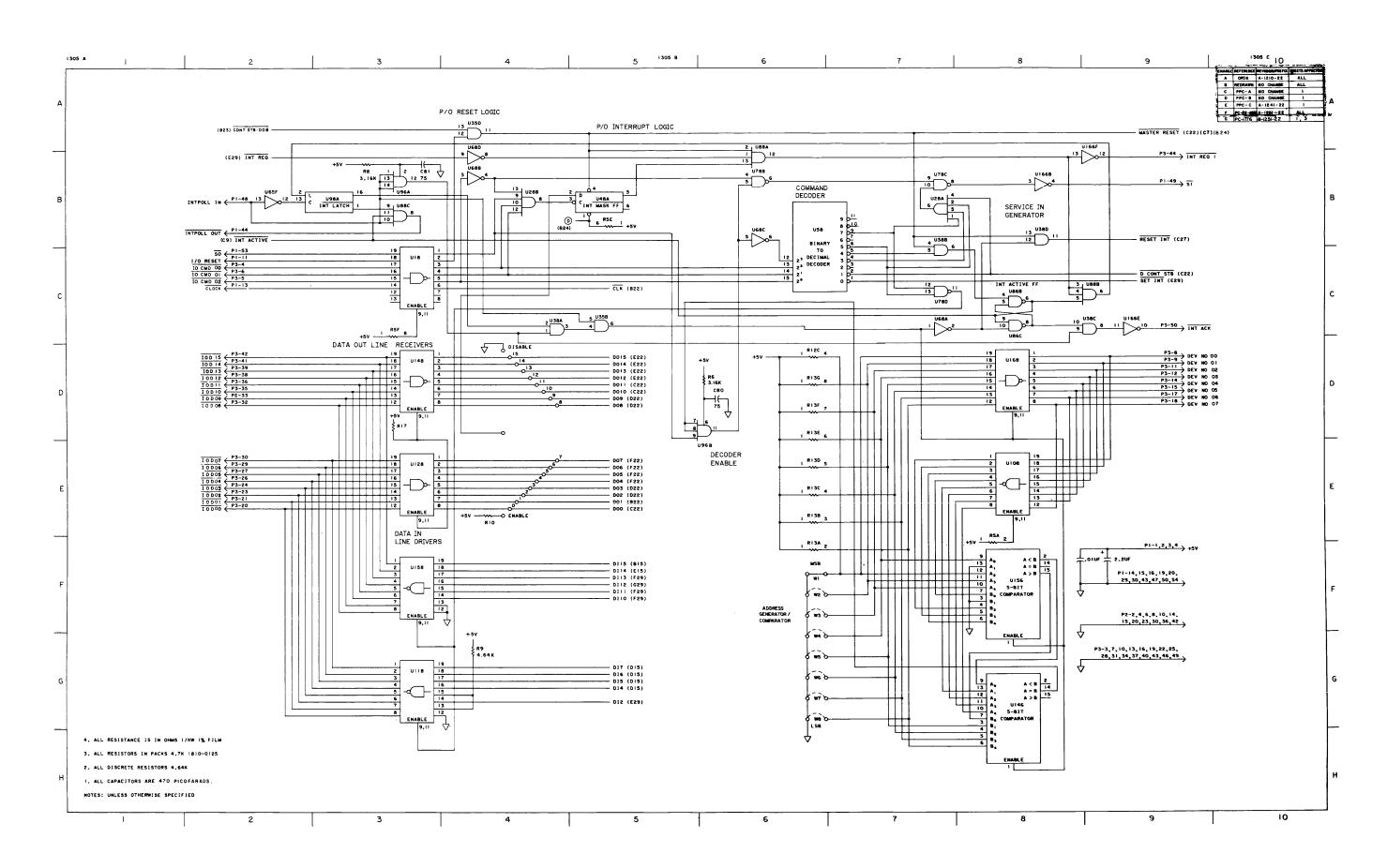




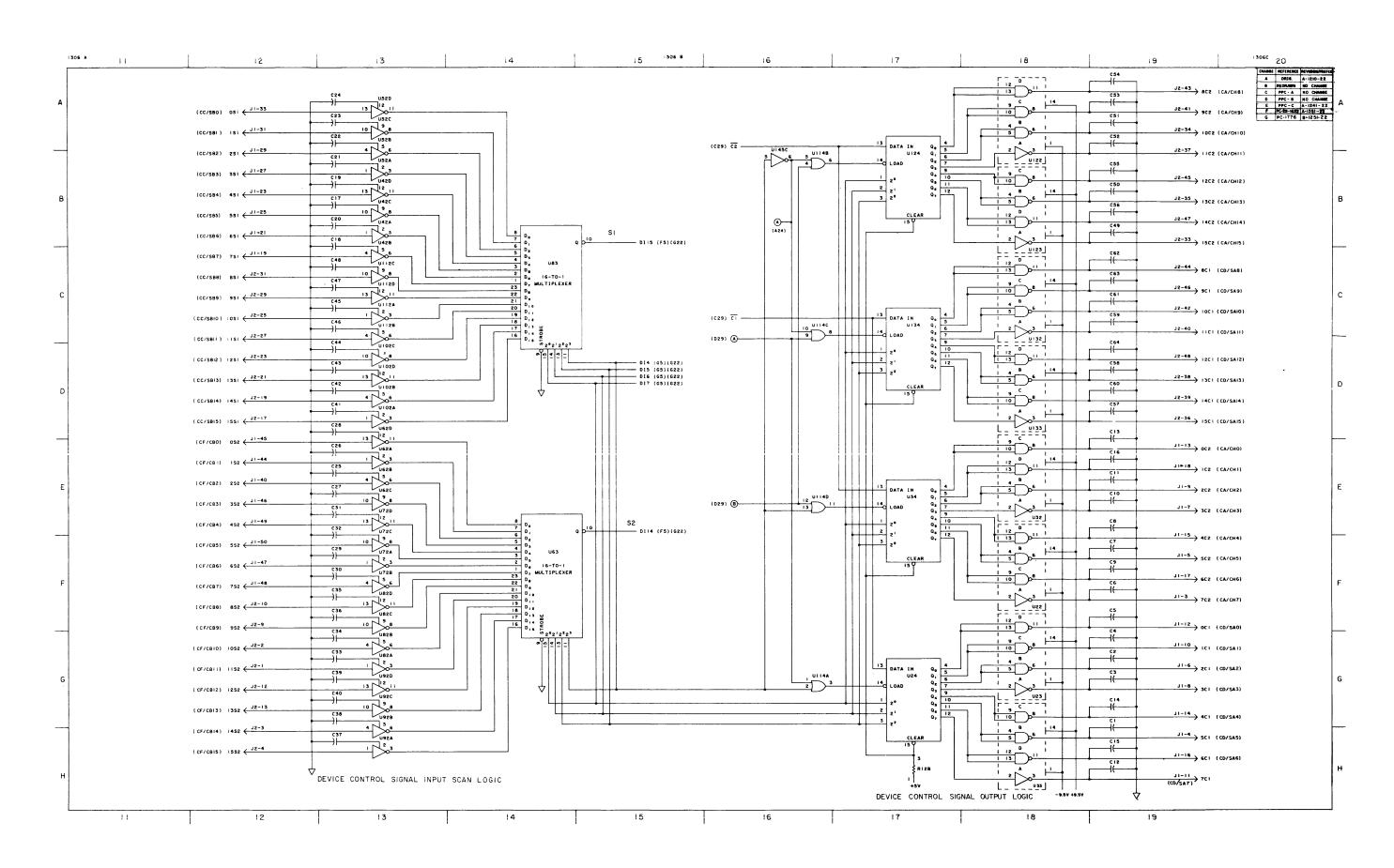


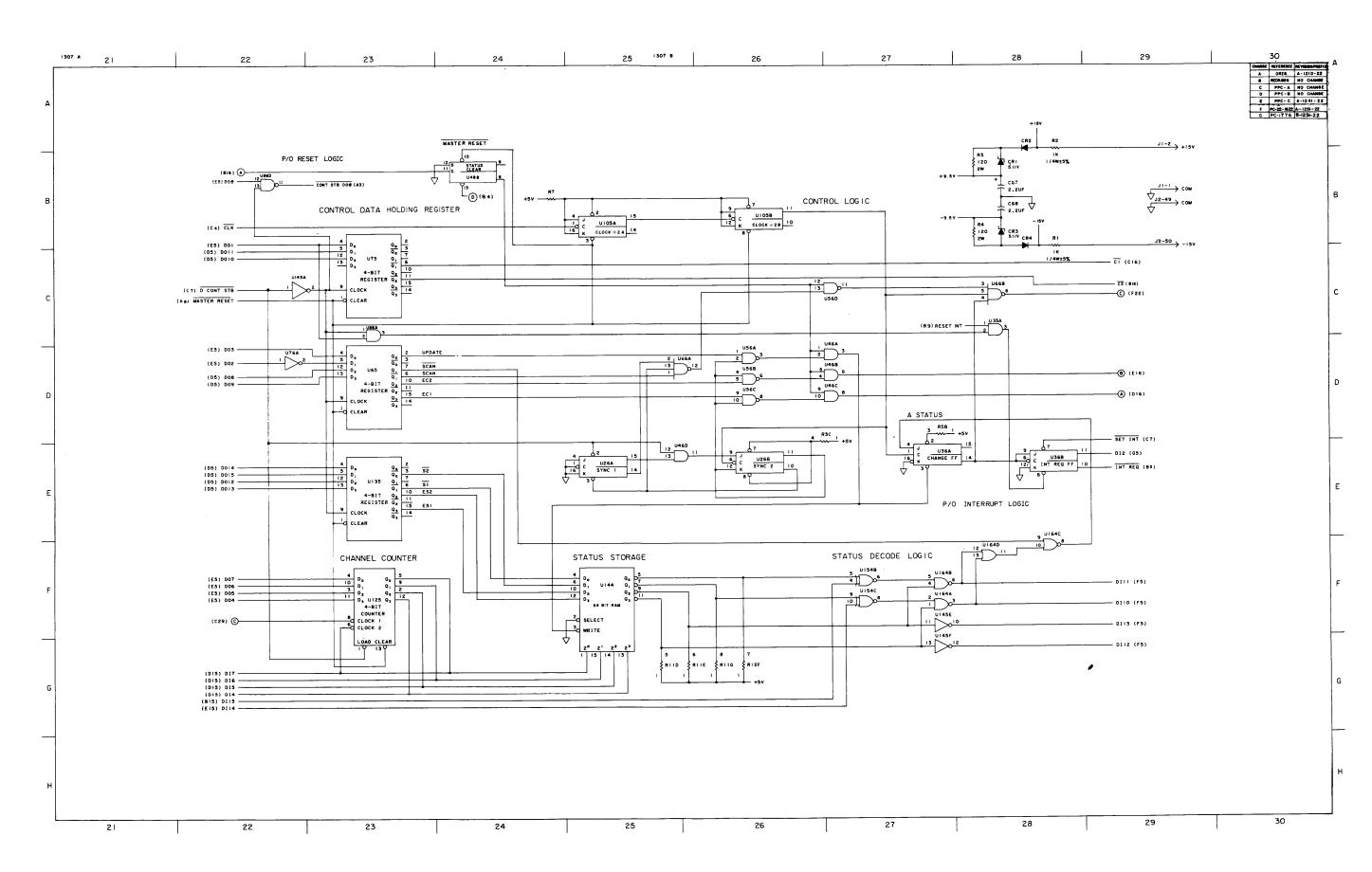


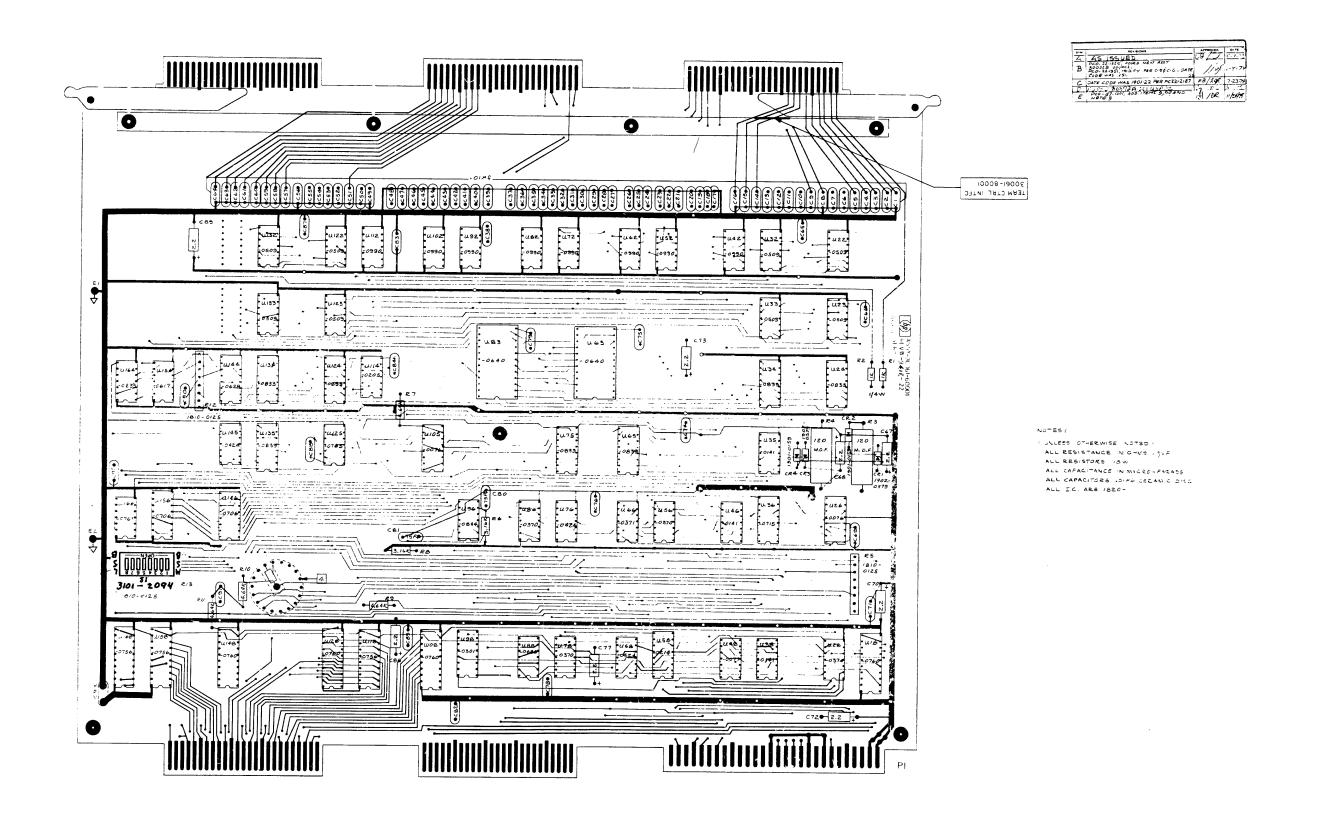


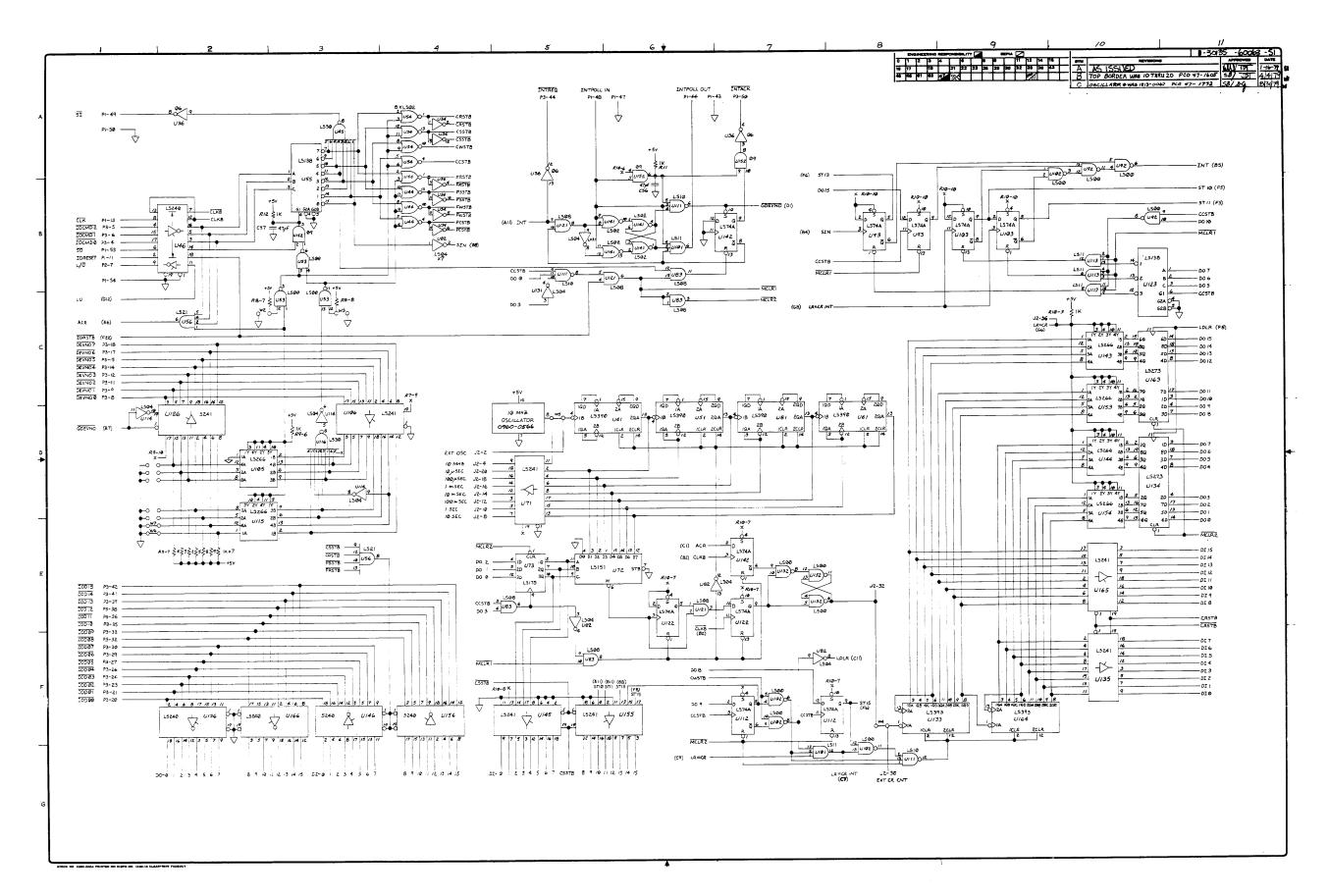


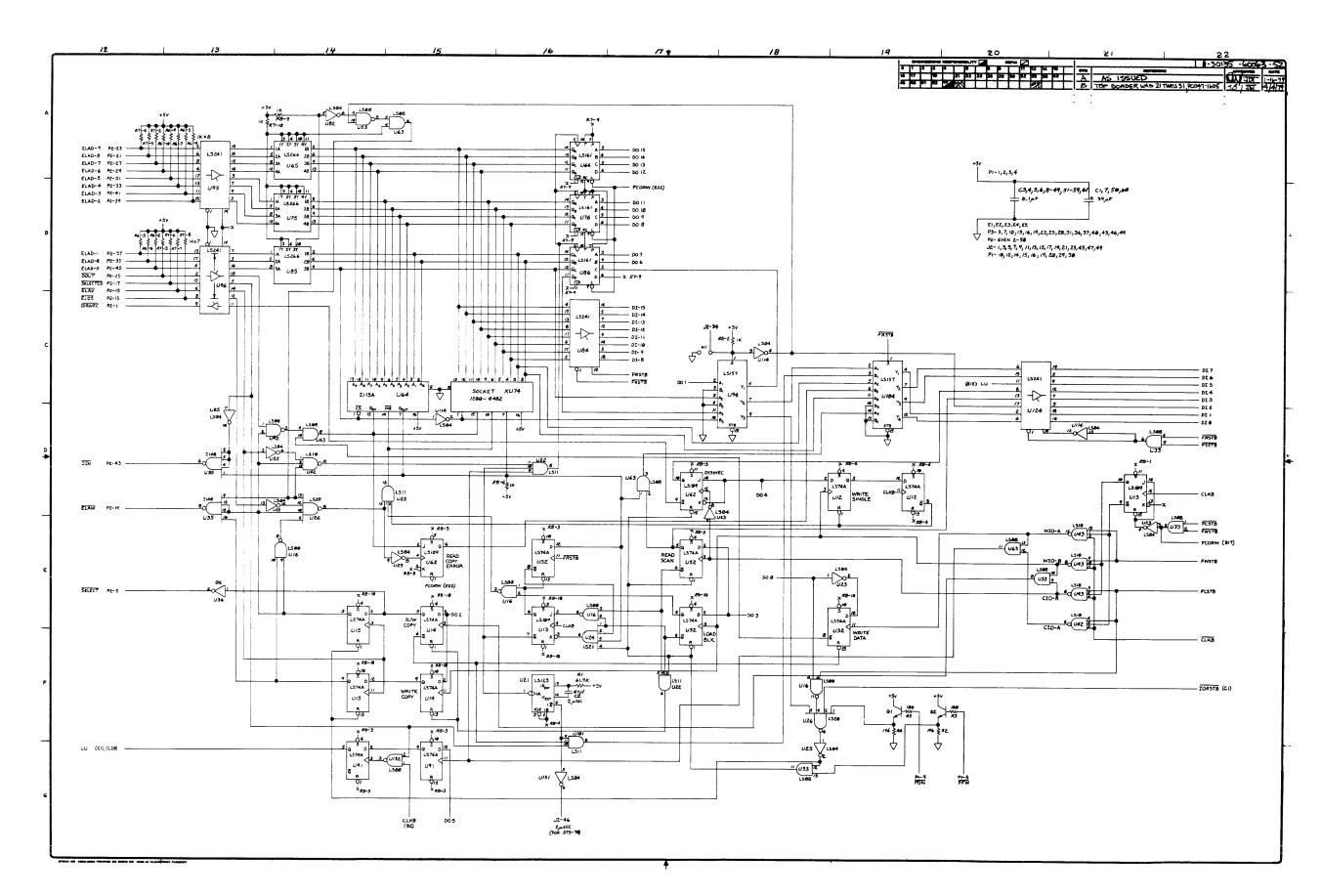
Terminal Control Interface PCA, 30061-60001, Sheet 1 of 4

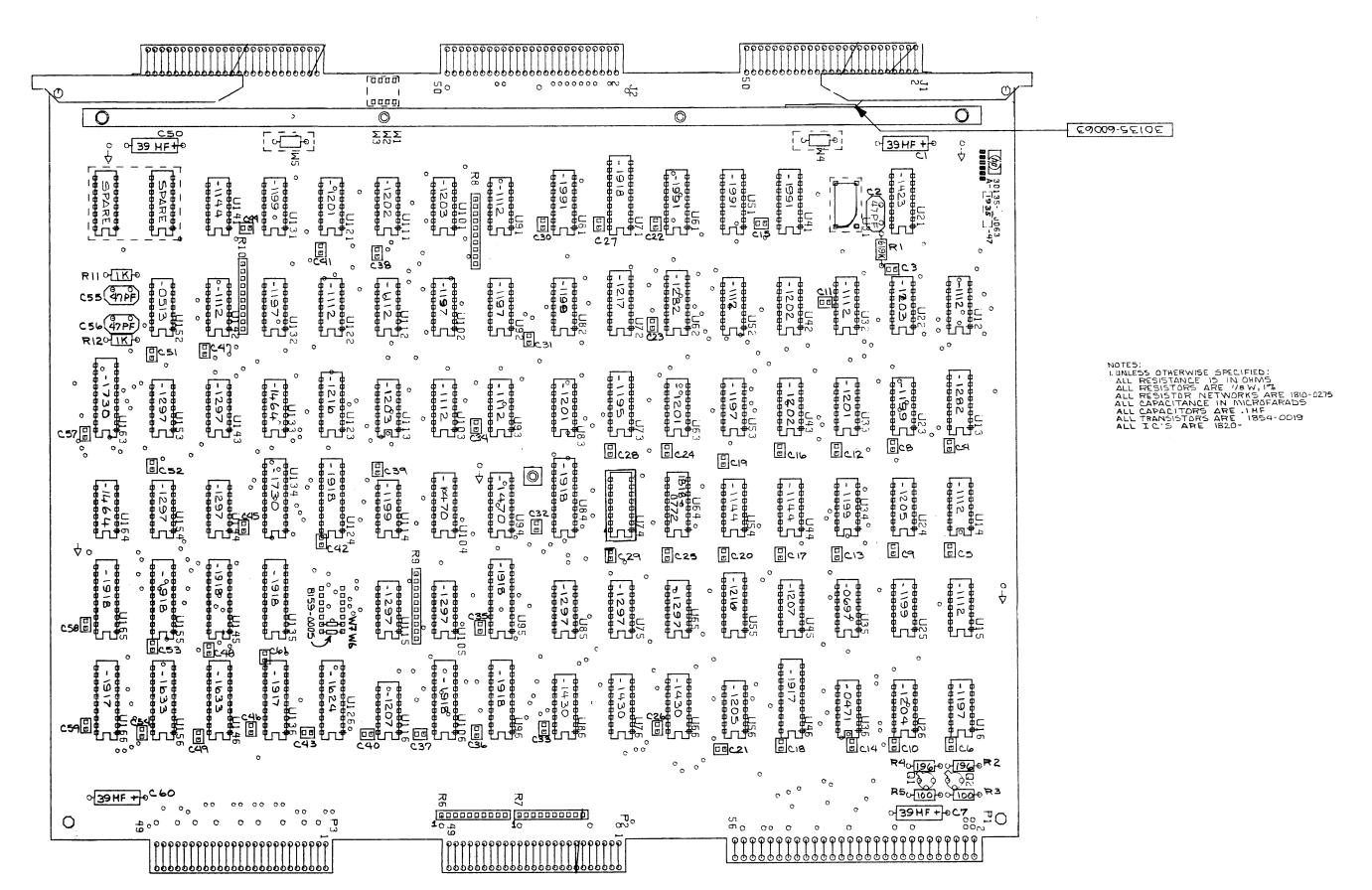


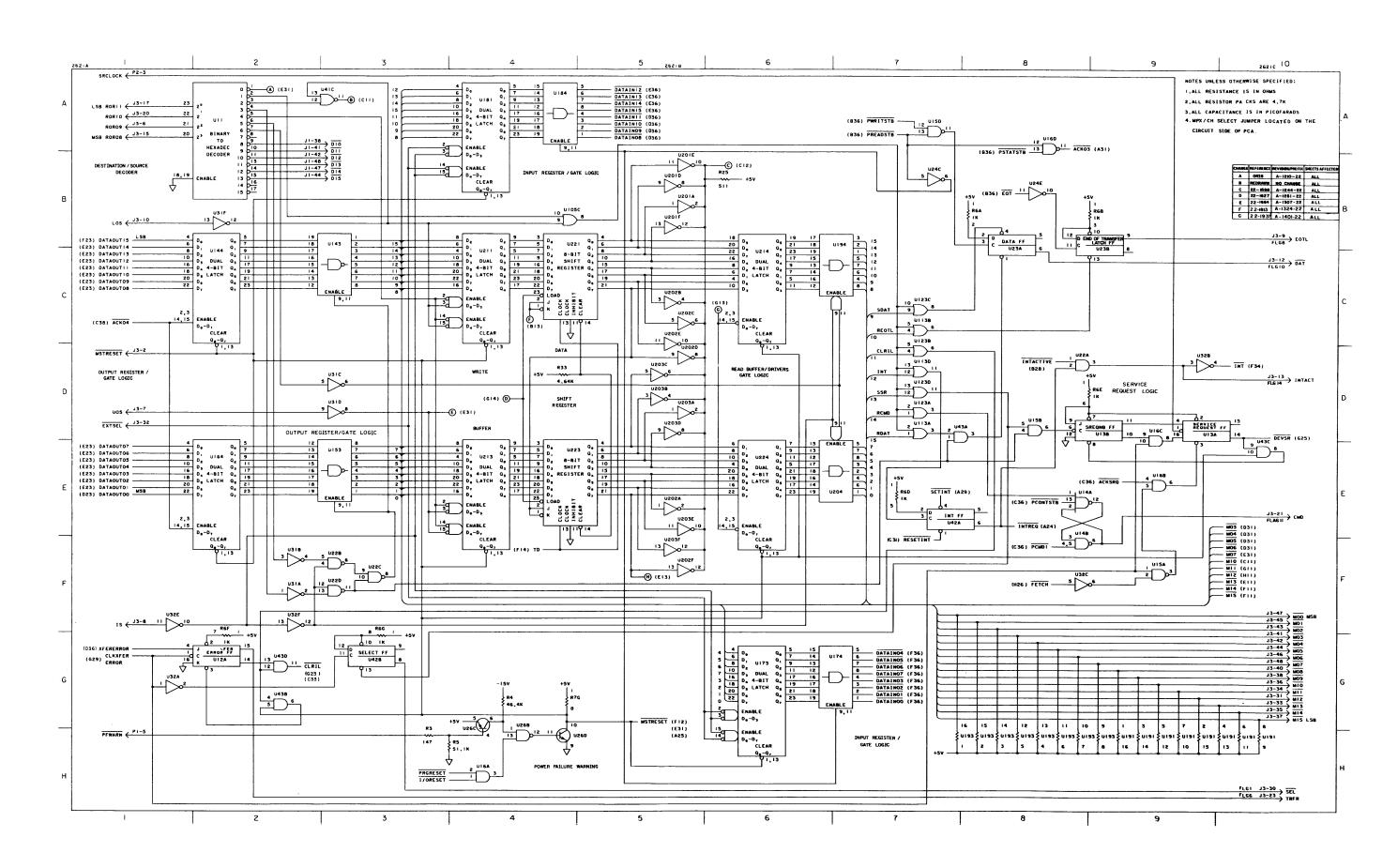


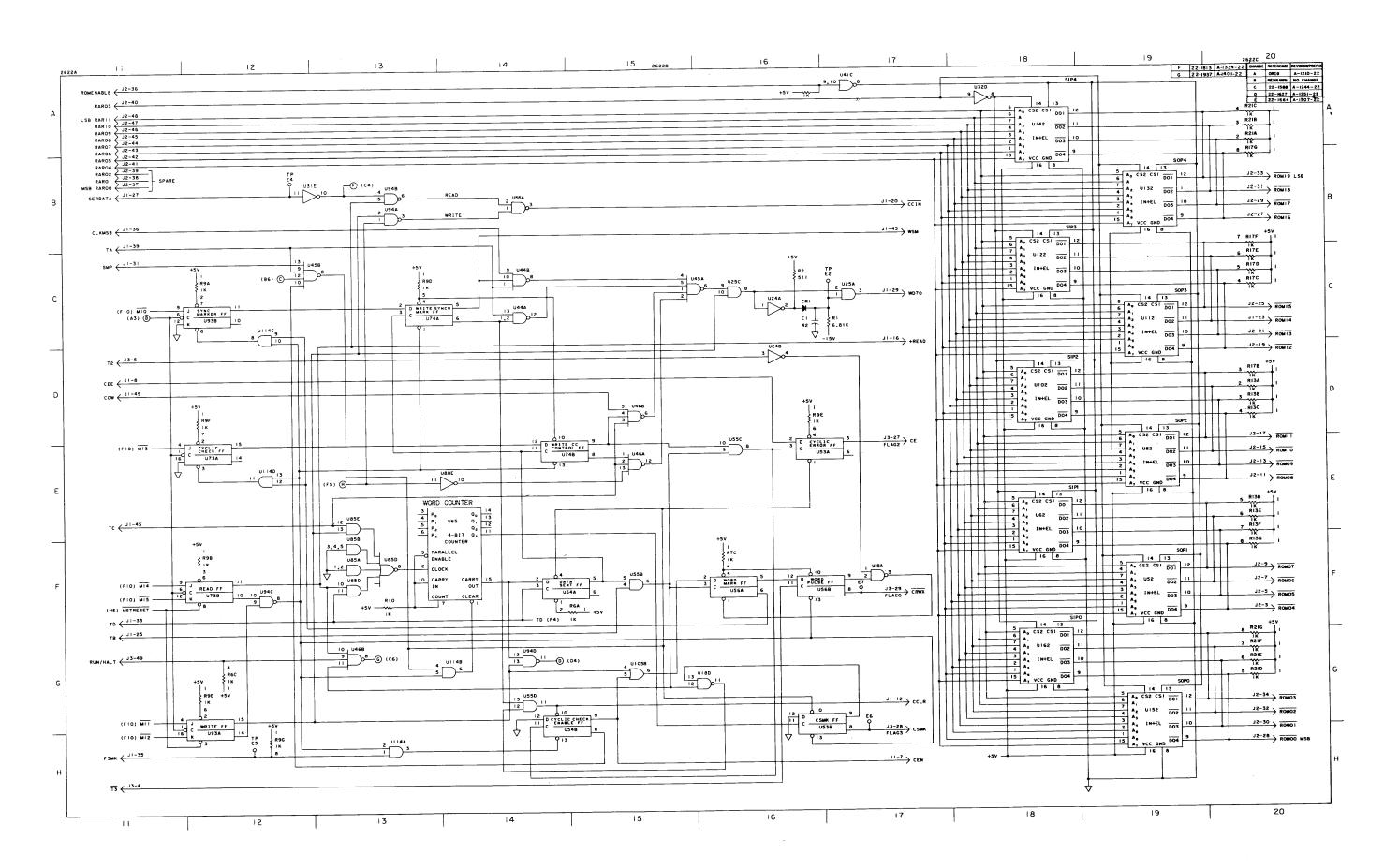


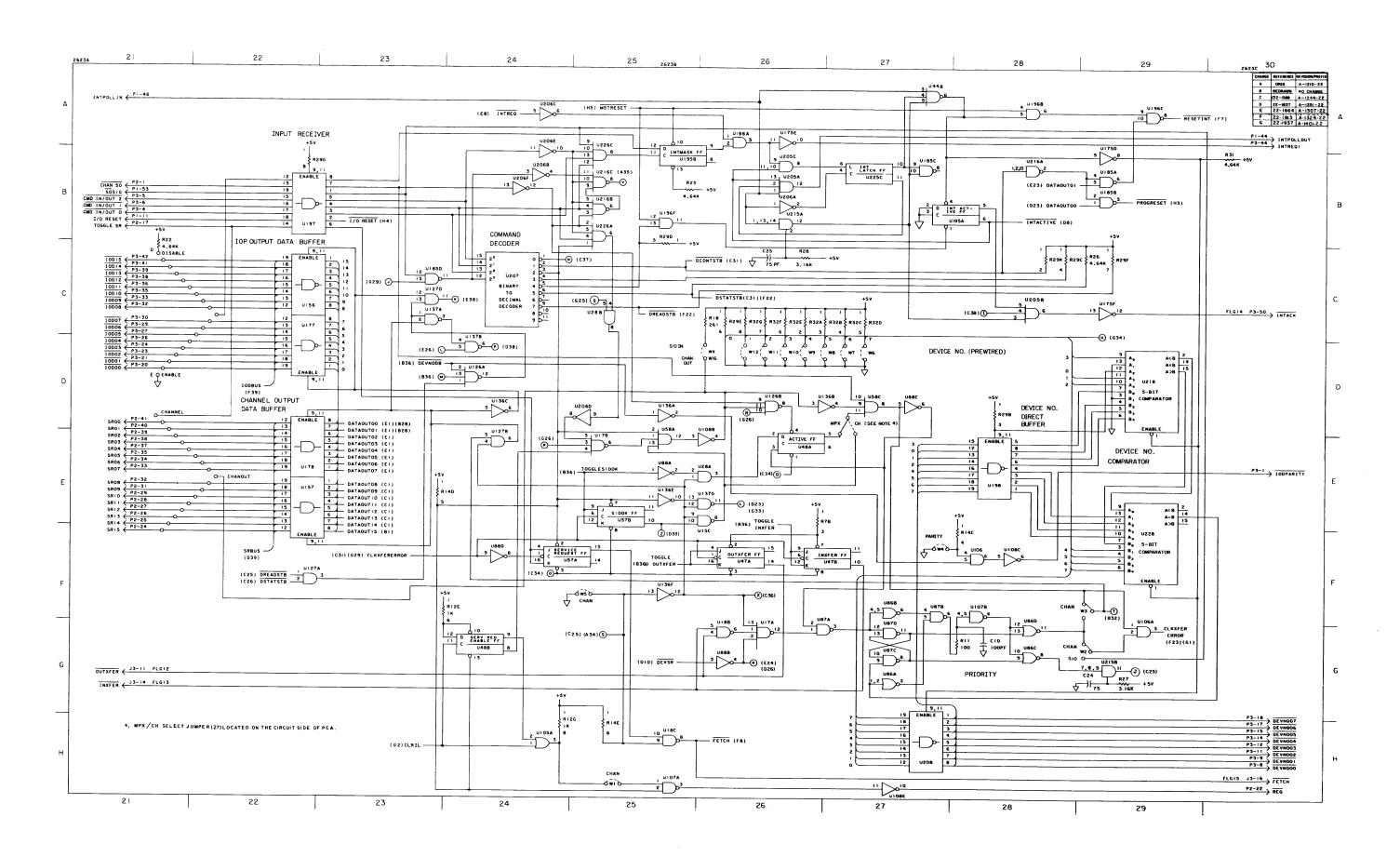


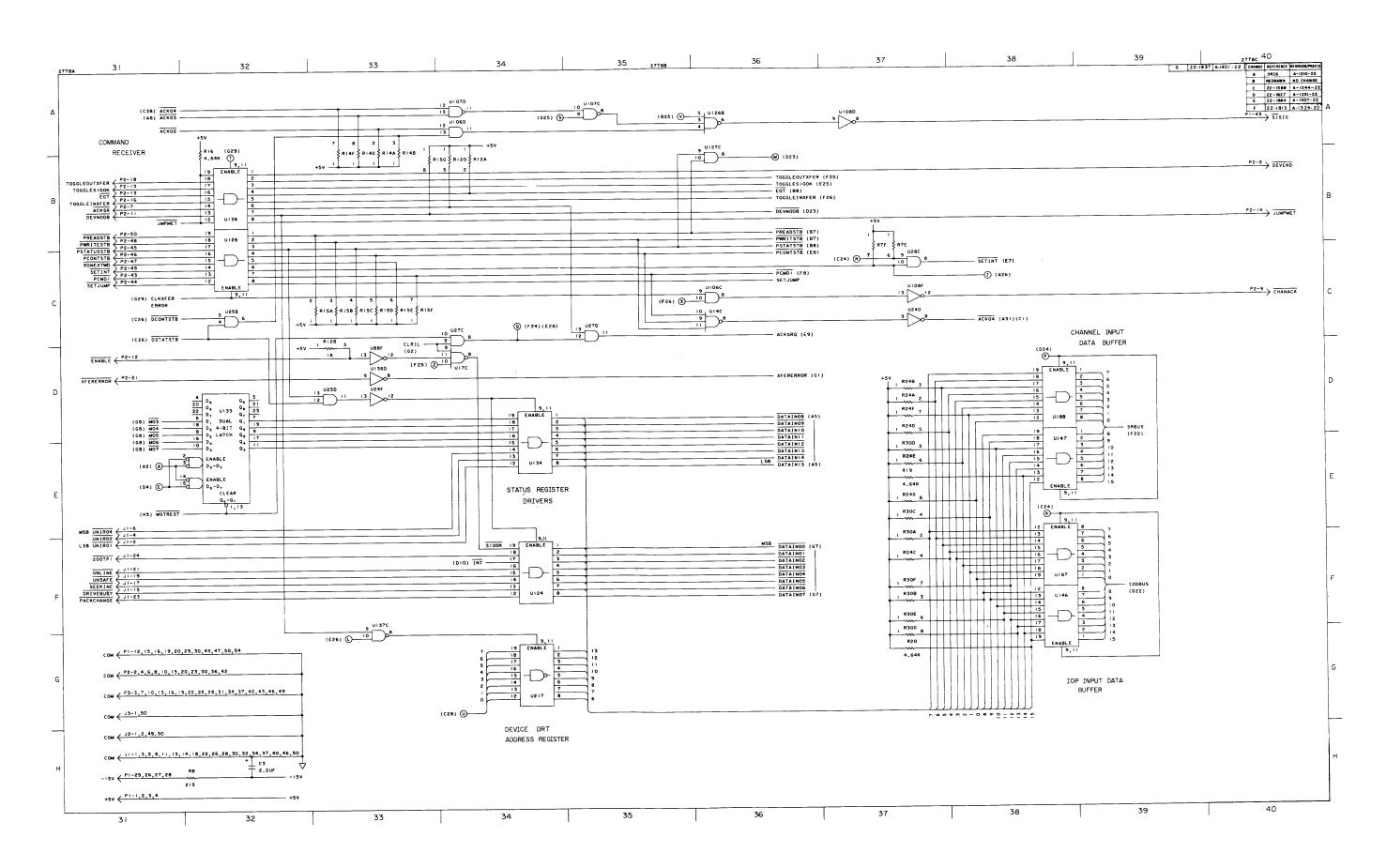


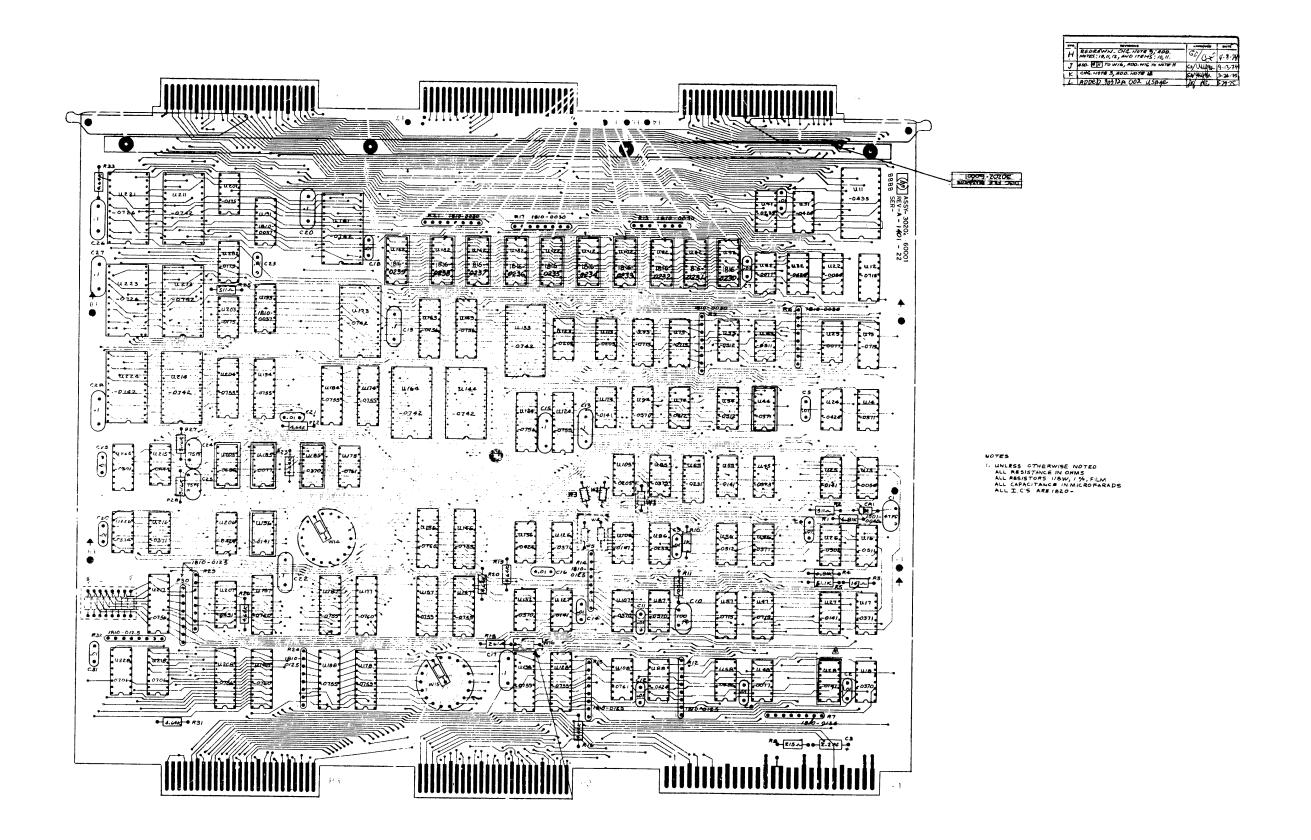


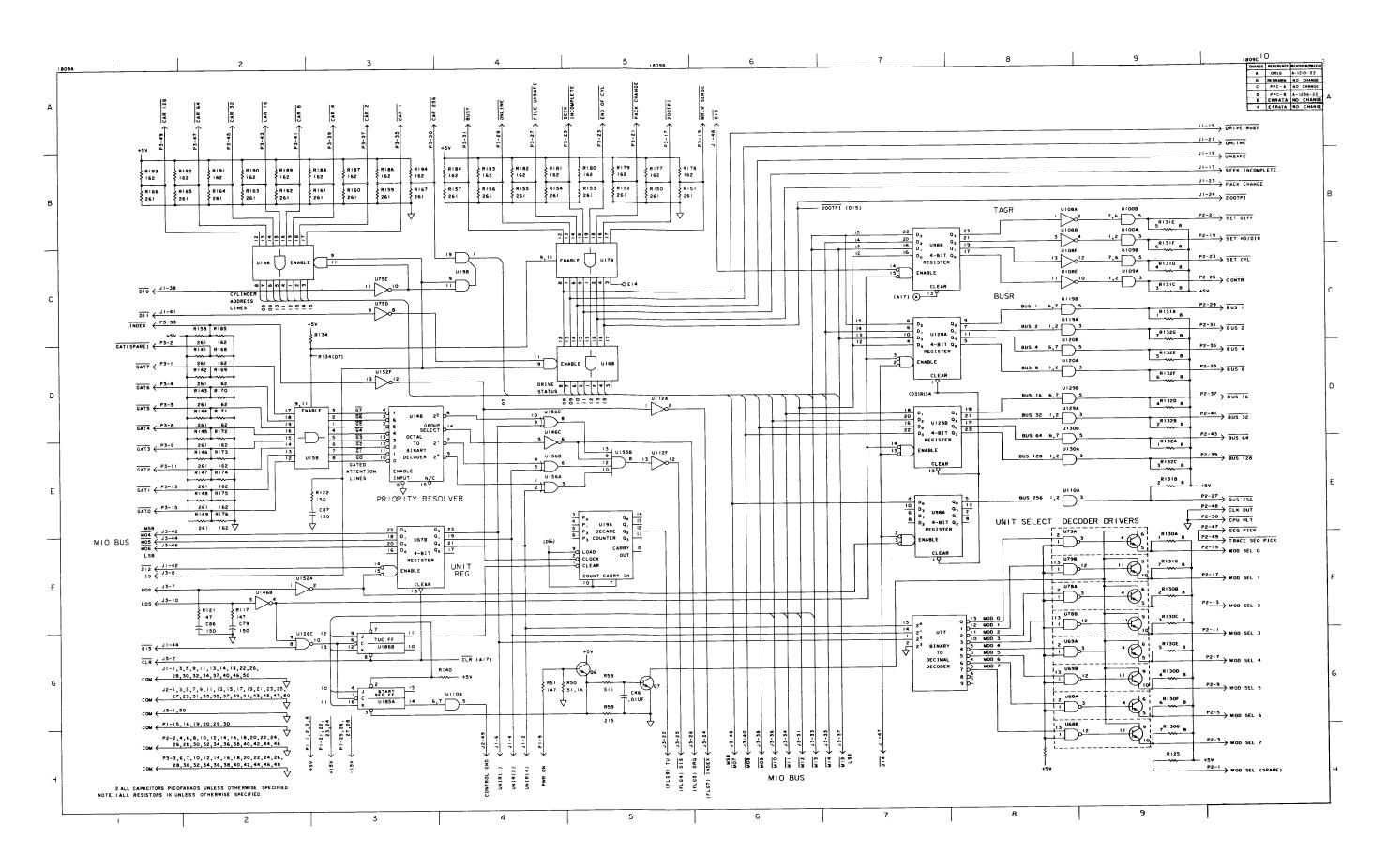


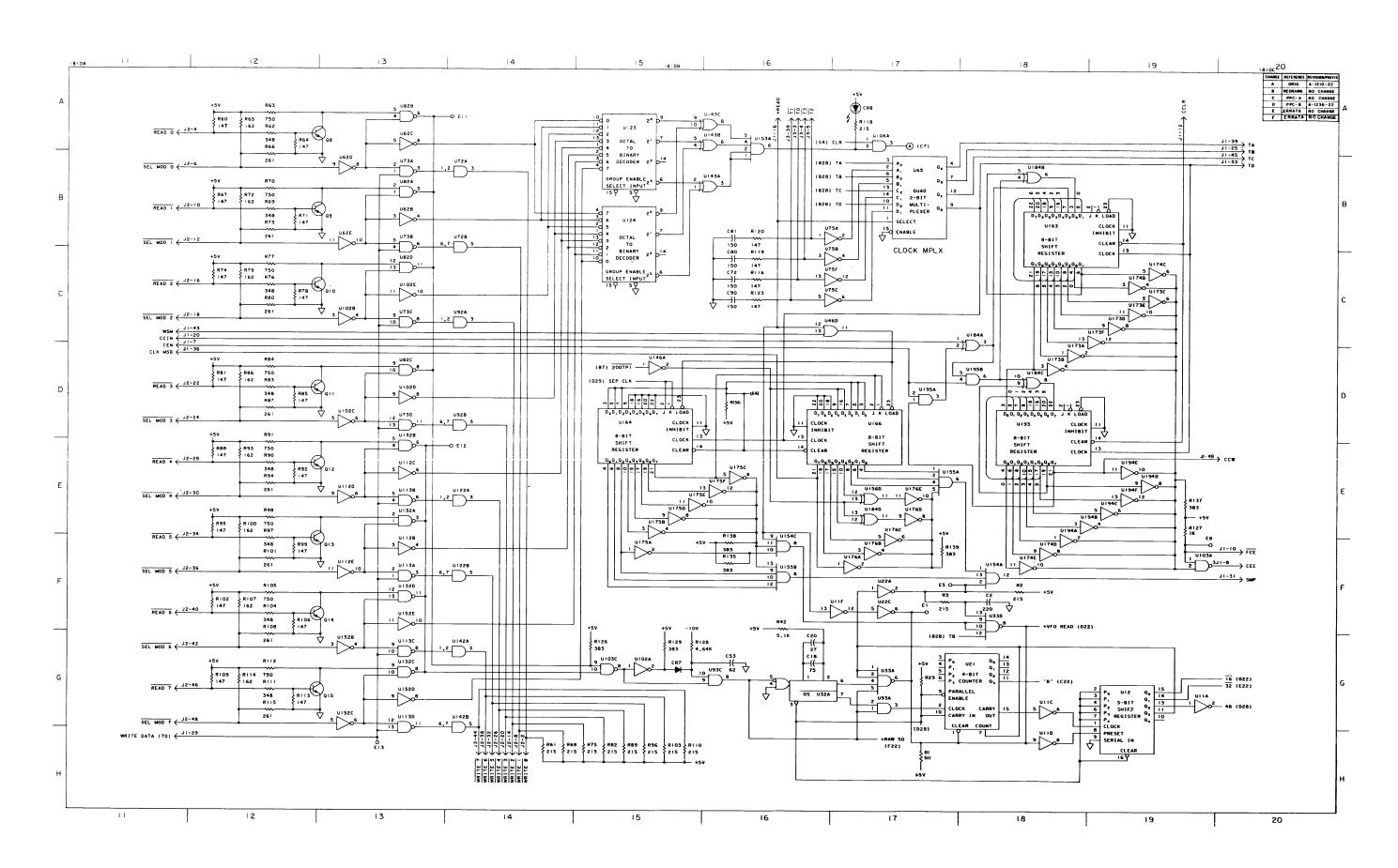


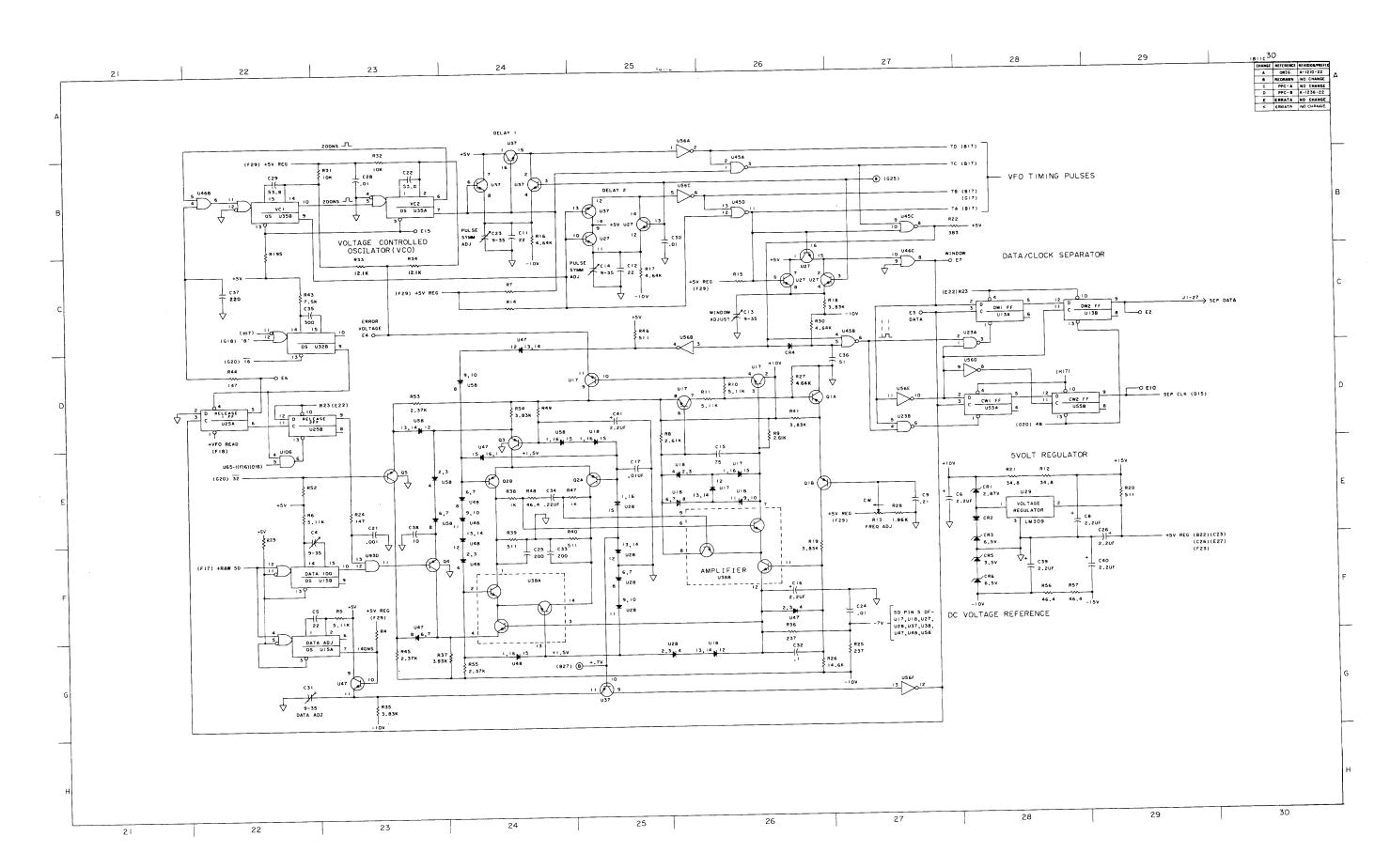


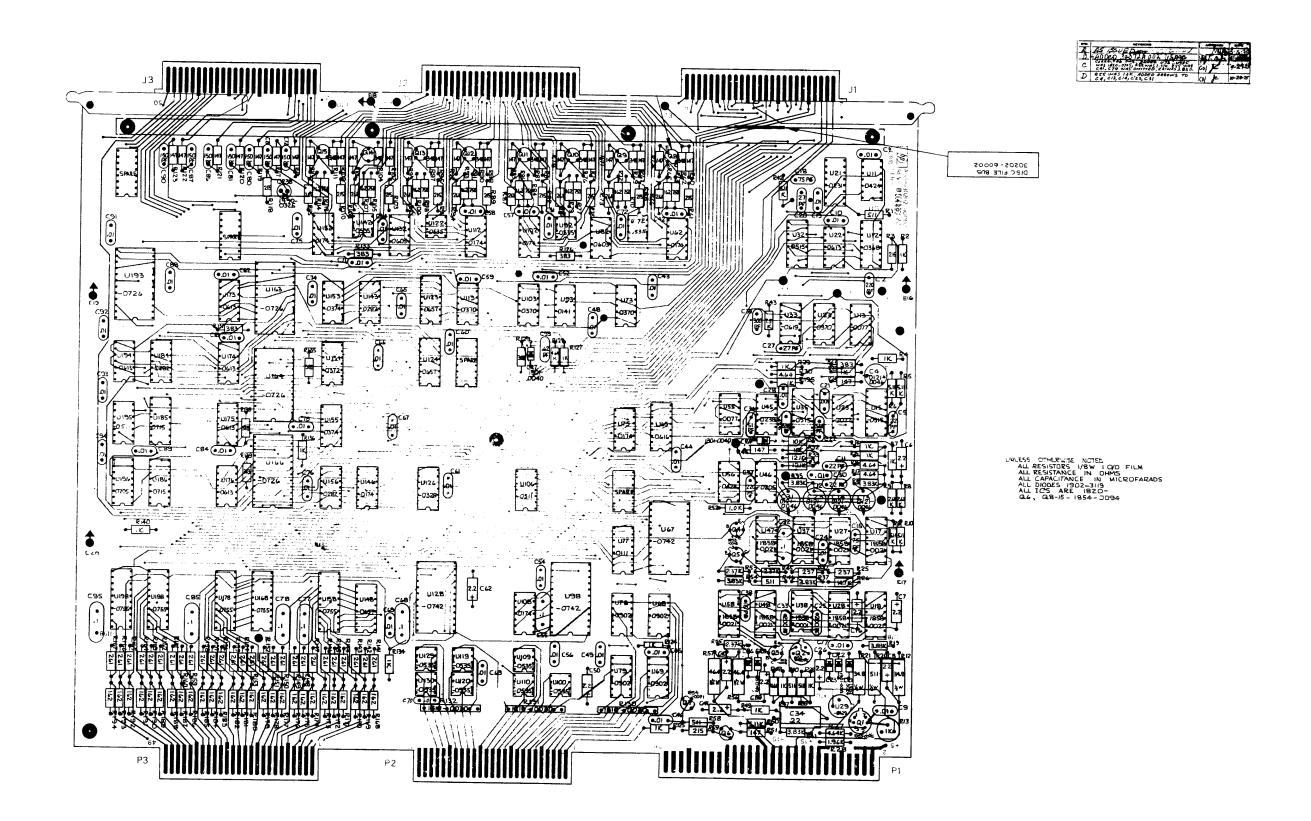


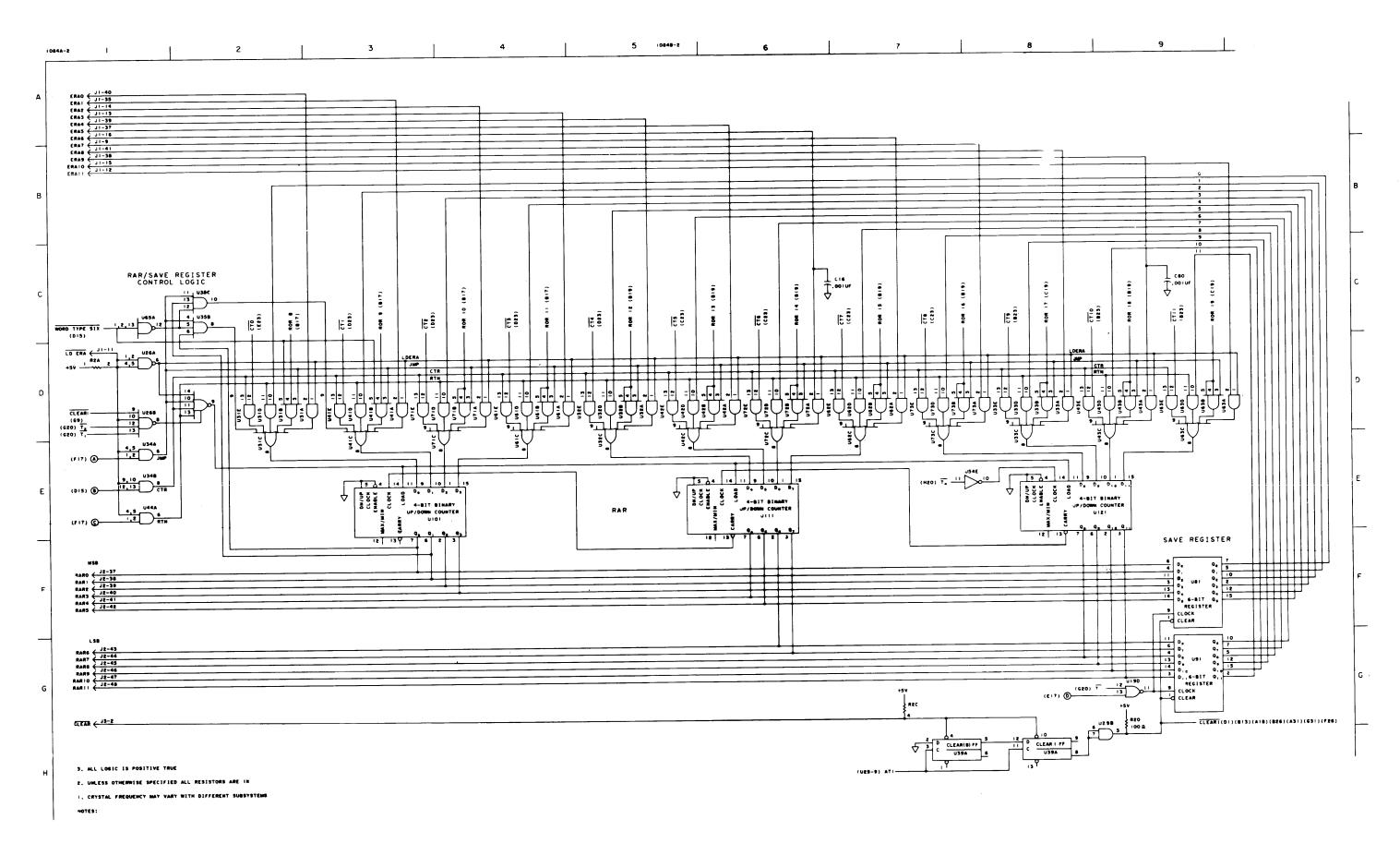


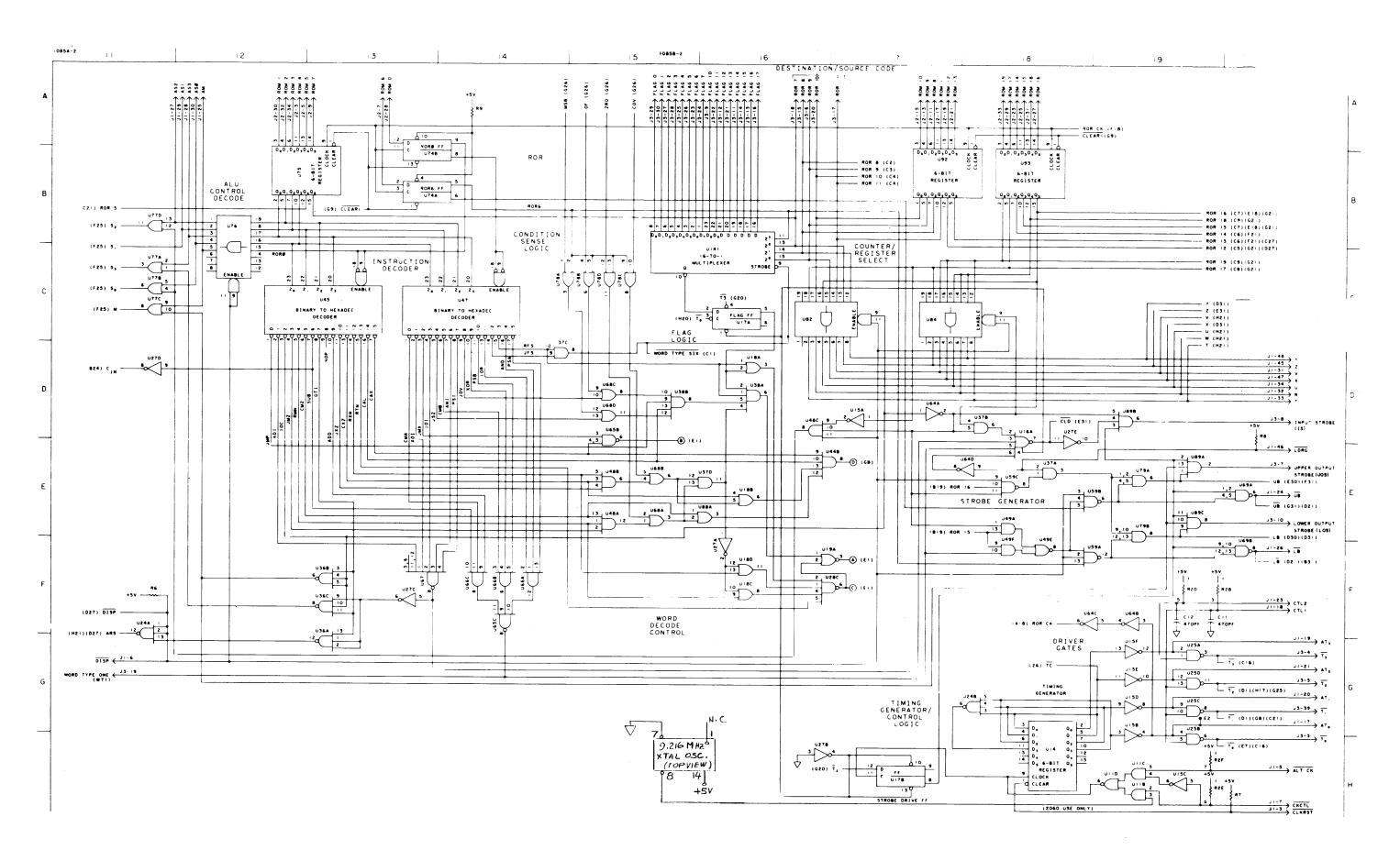




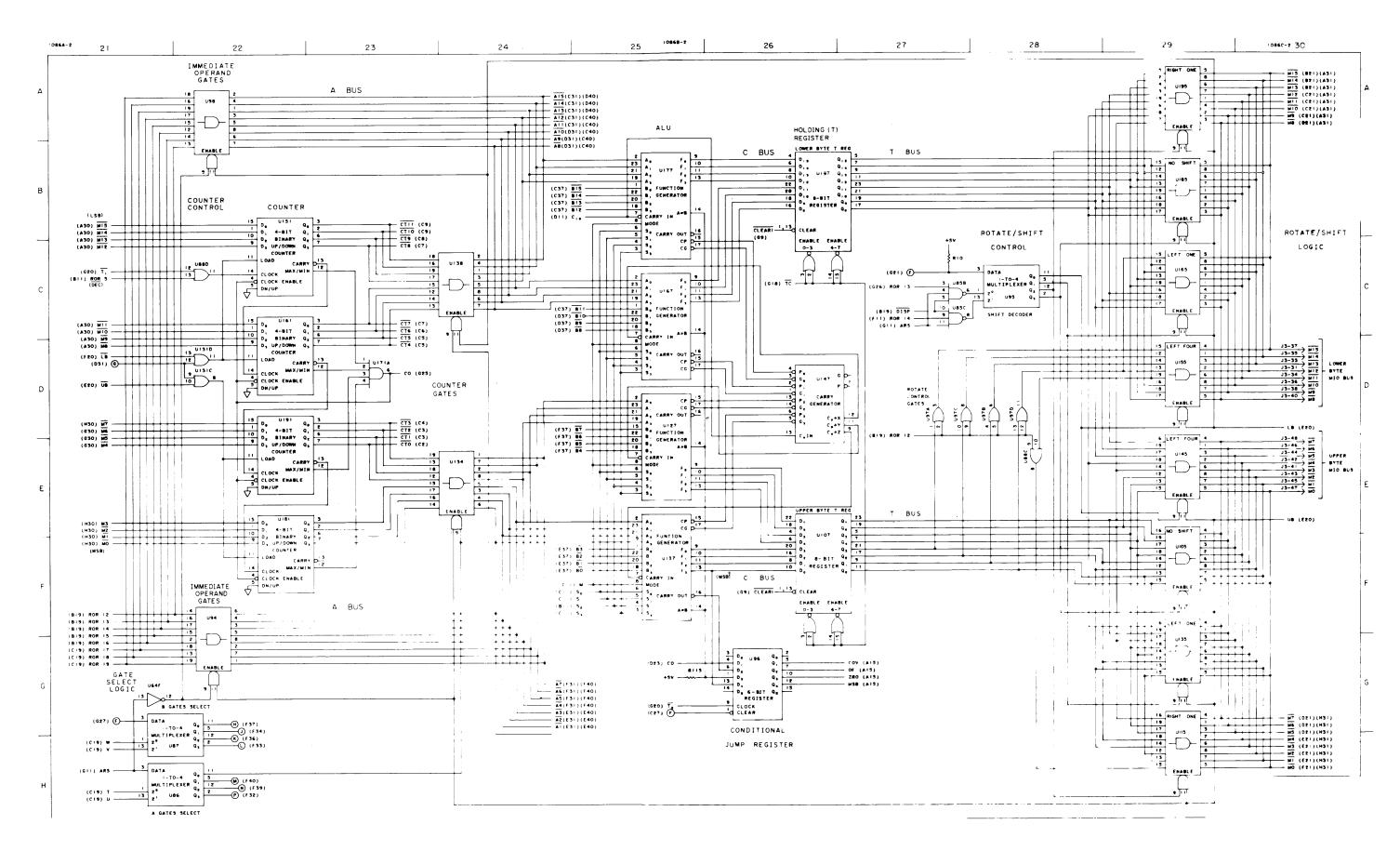


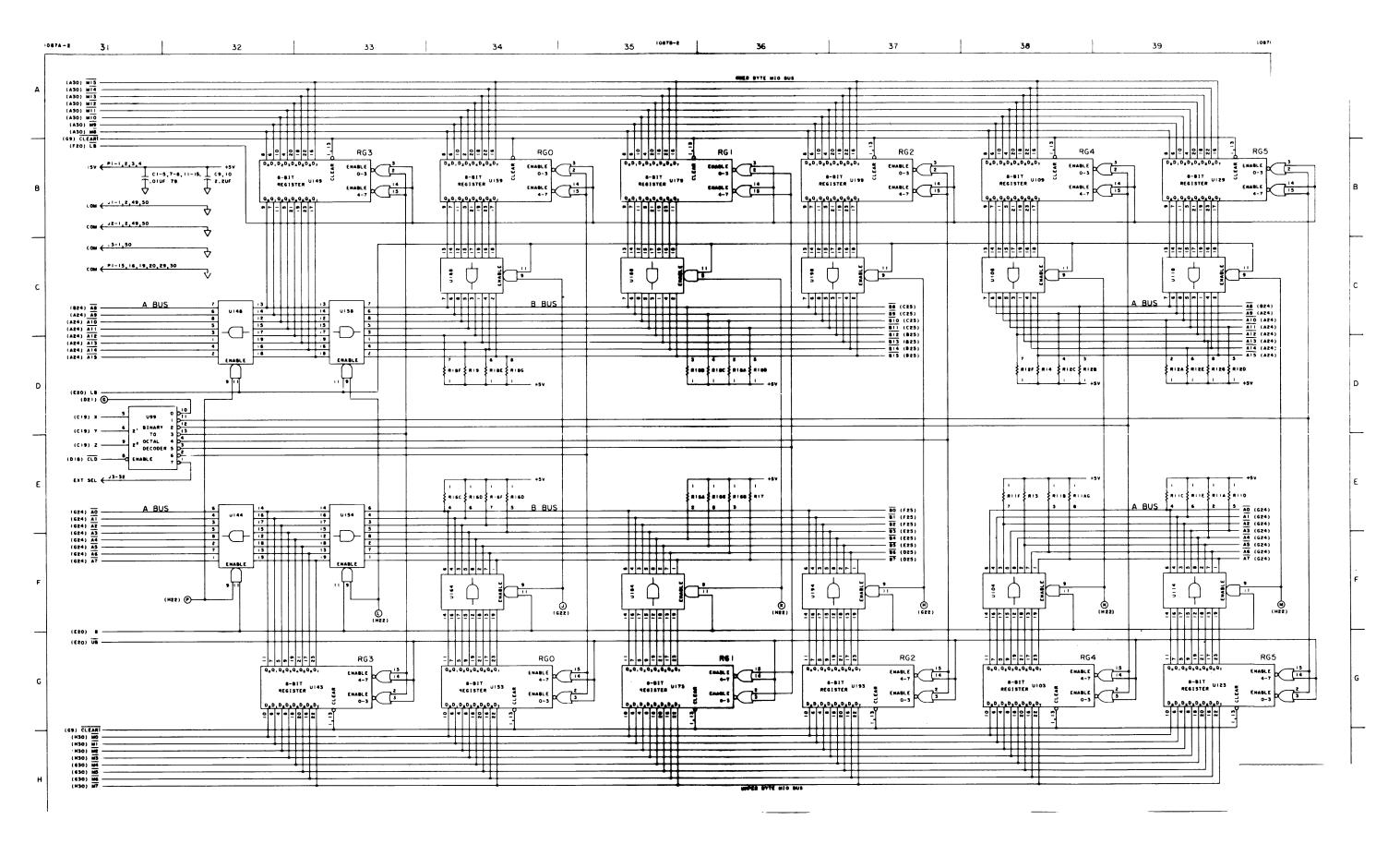




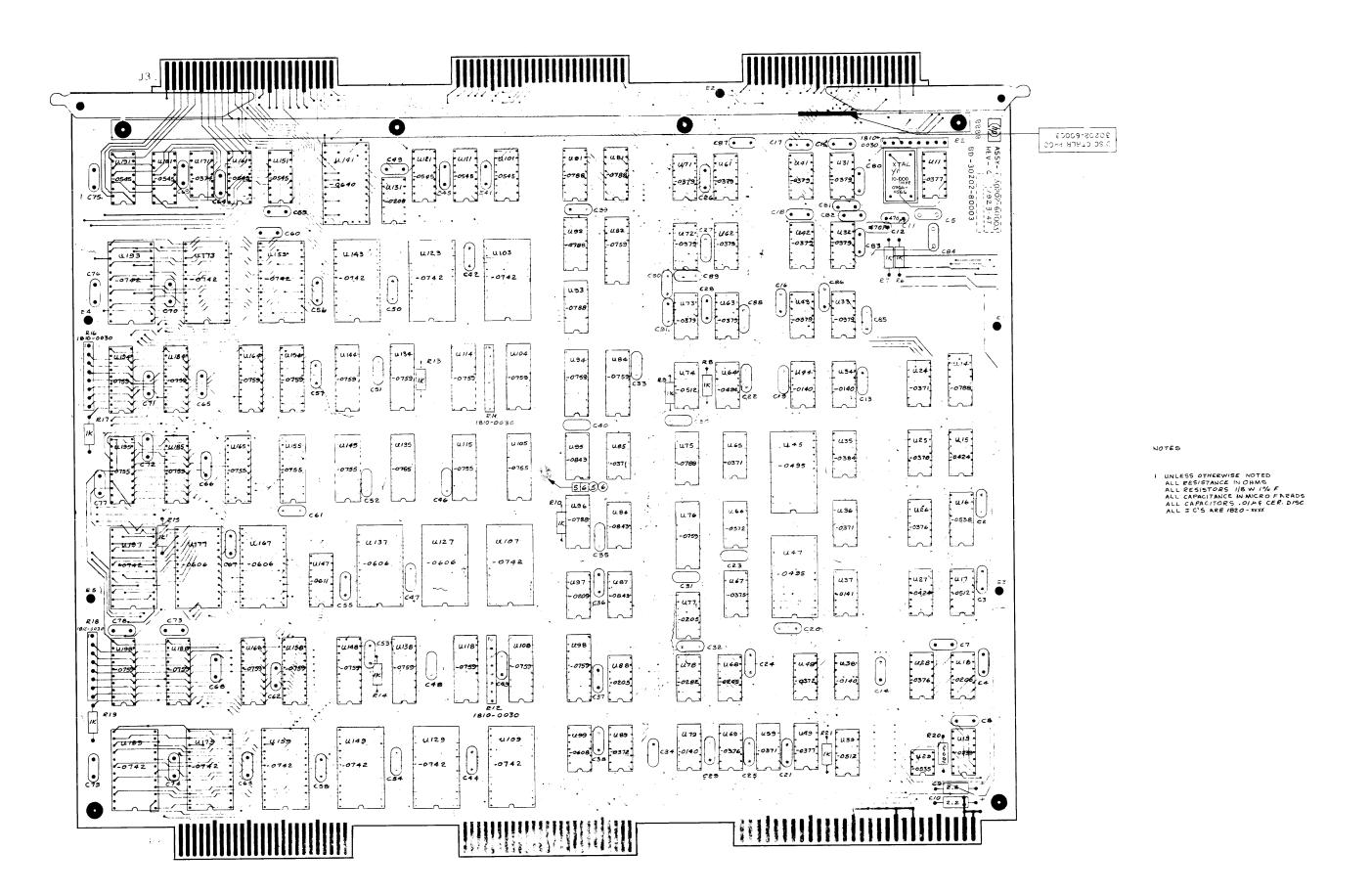


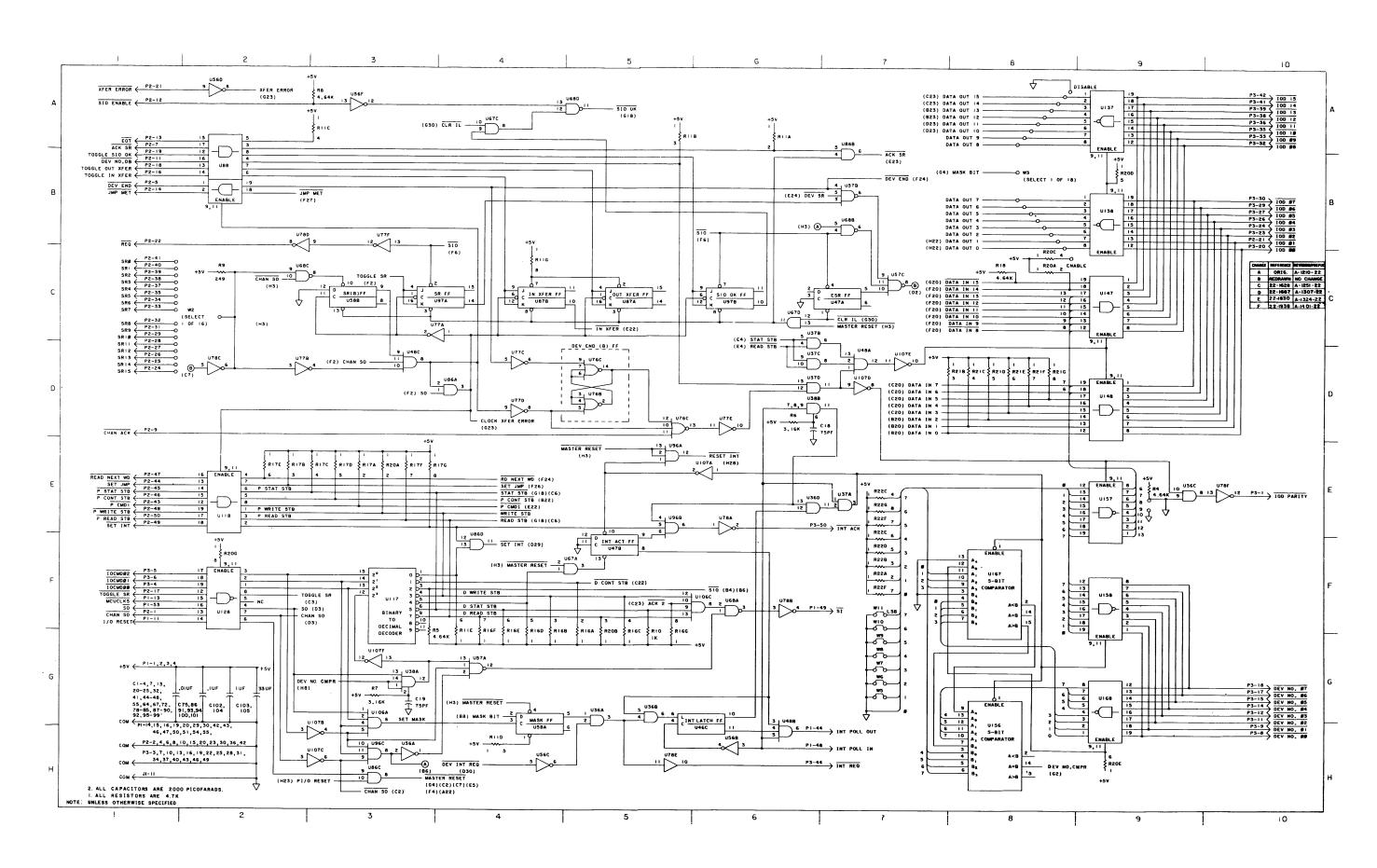
Disc Controller Processor PCA, 30202-60003, Sheet 2 of 5



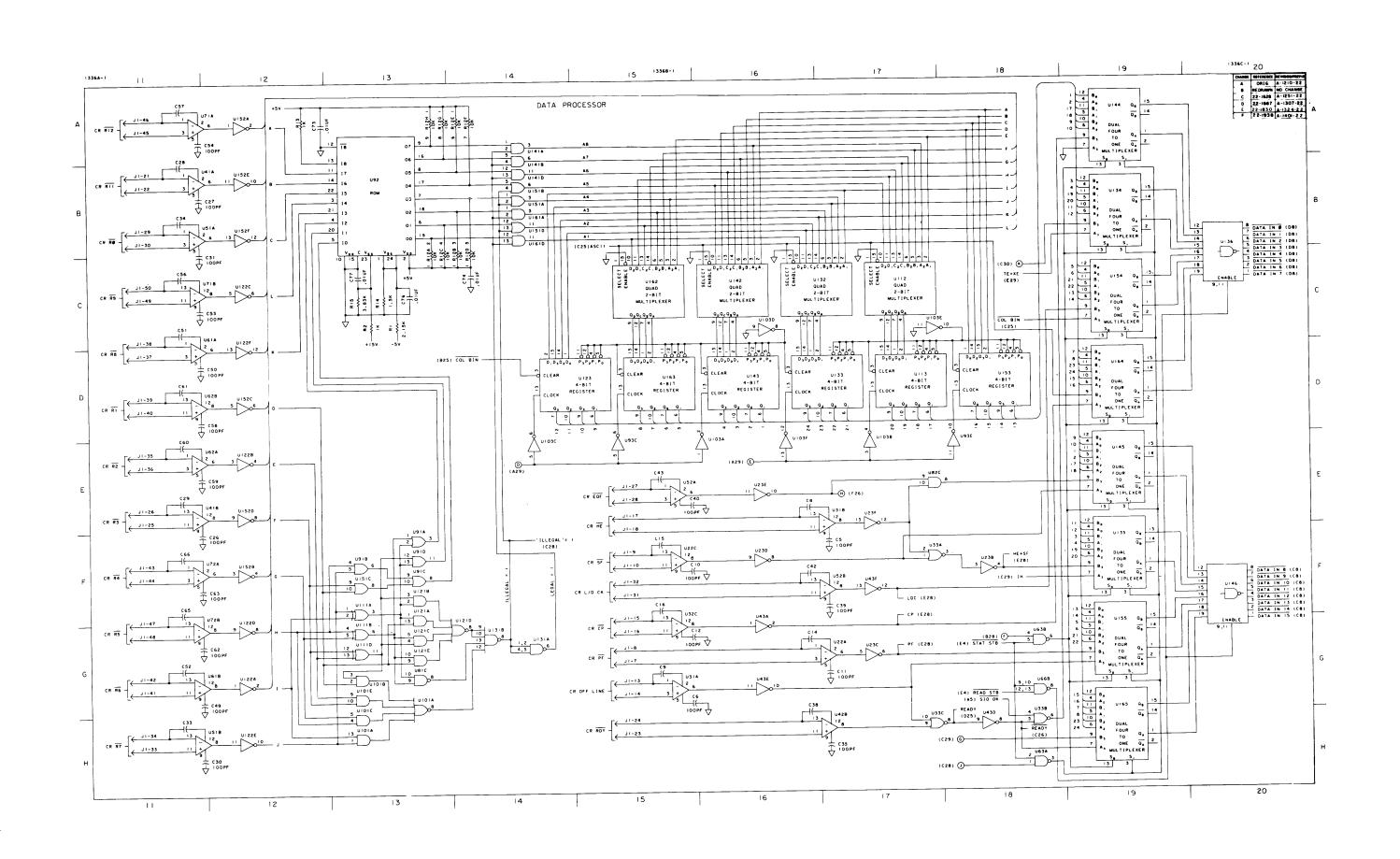


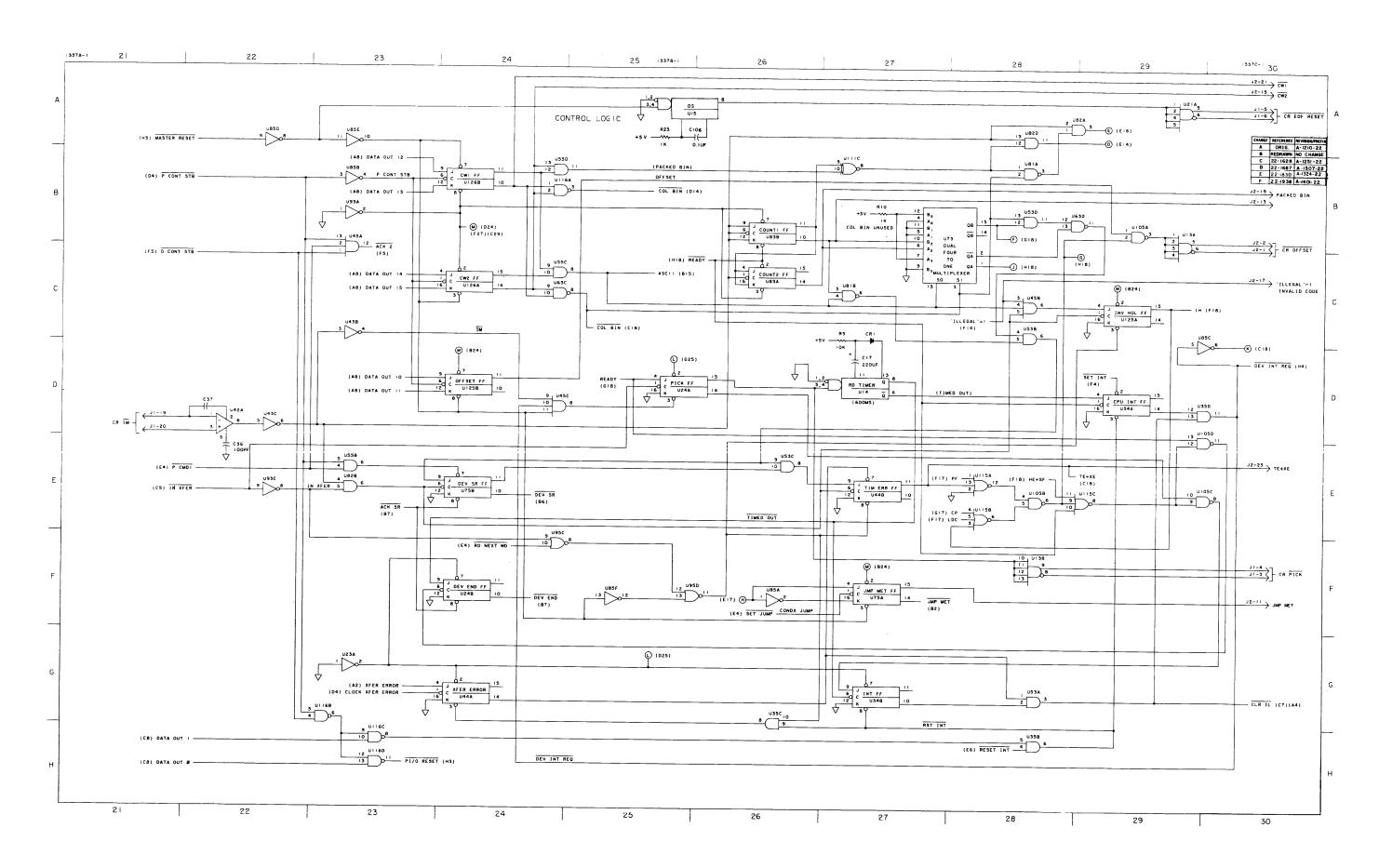
Disc Controller Processor PCA, 30202-60003, Sheet 4 of 5

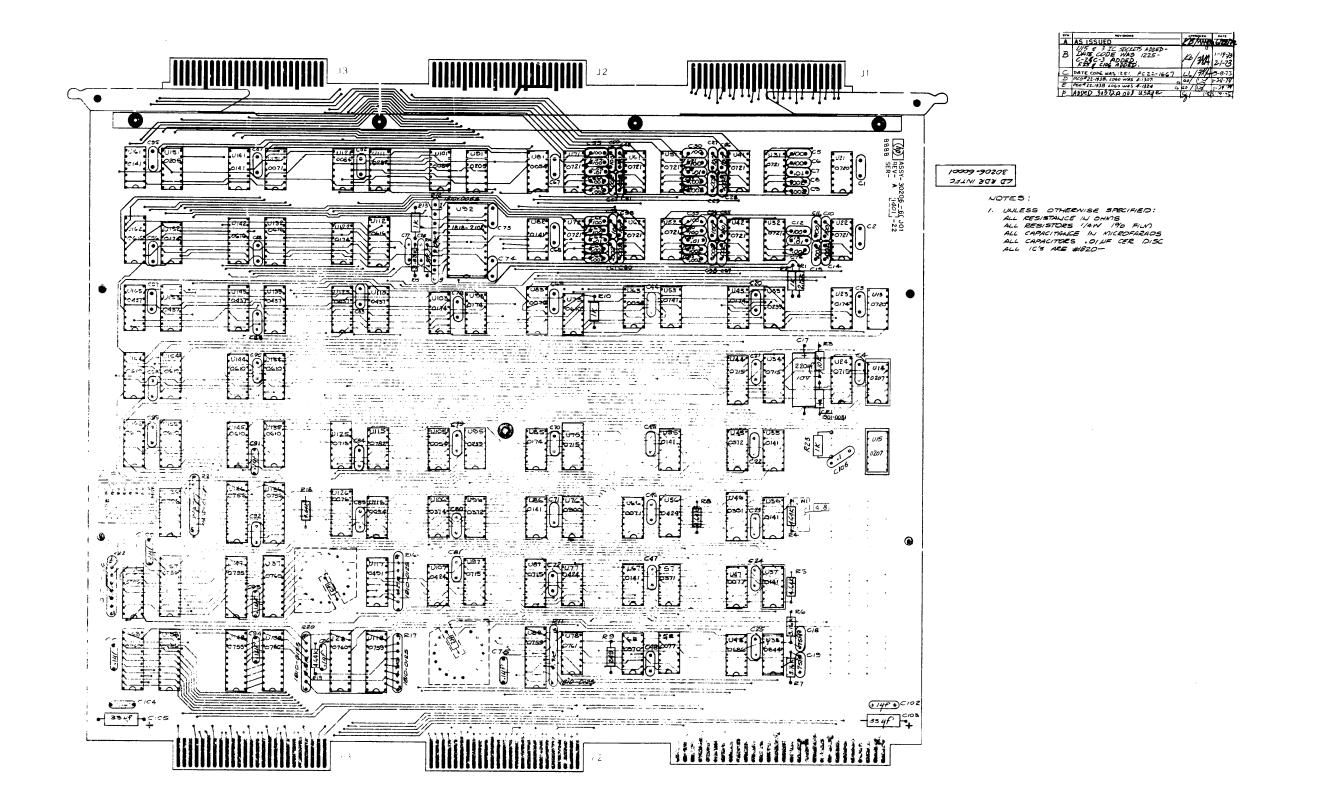


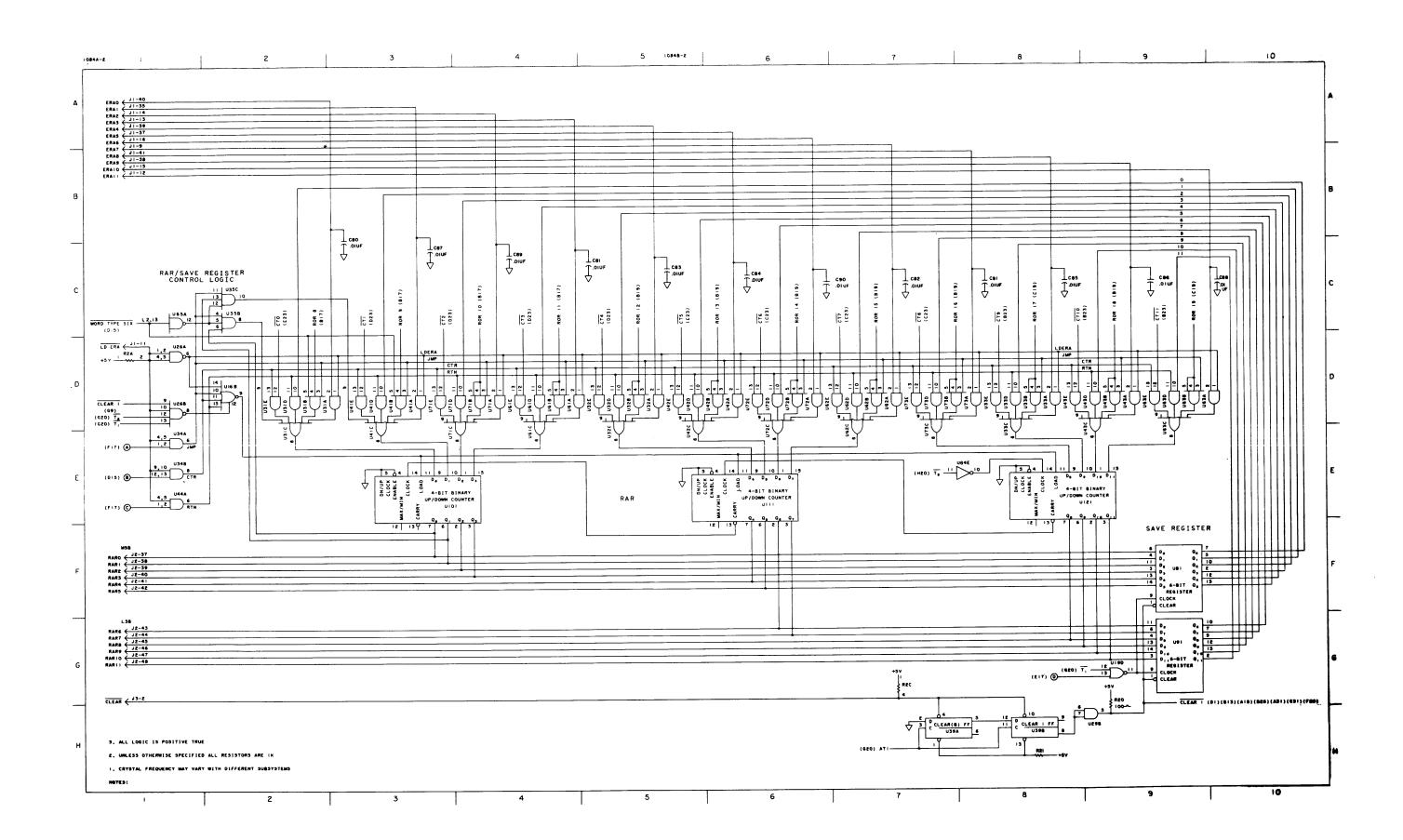


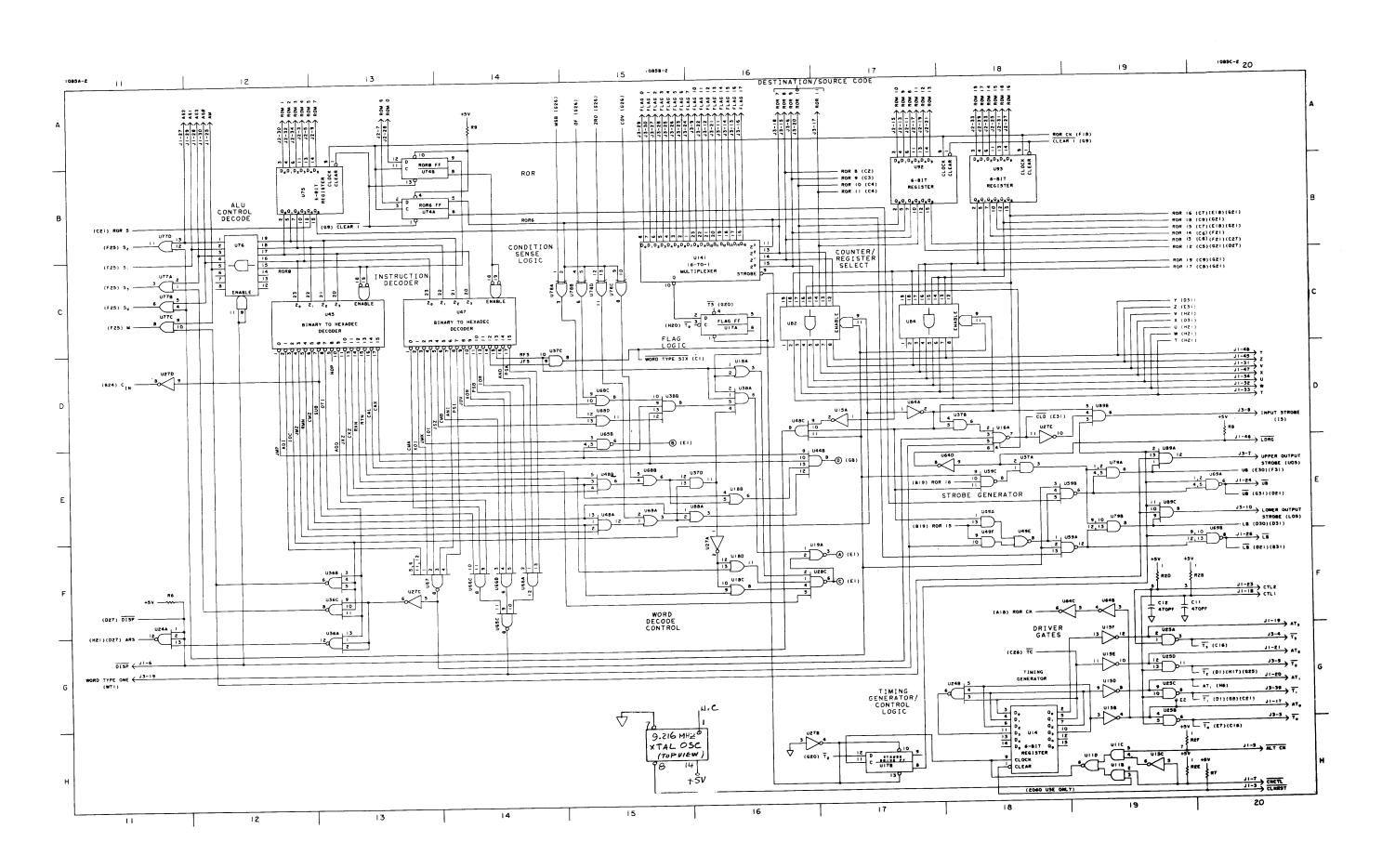
Card Reader Interface PCA, 30206-60001, Sheet 1 of 4

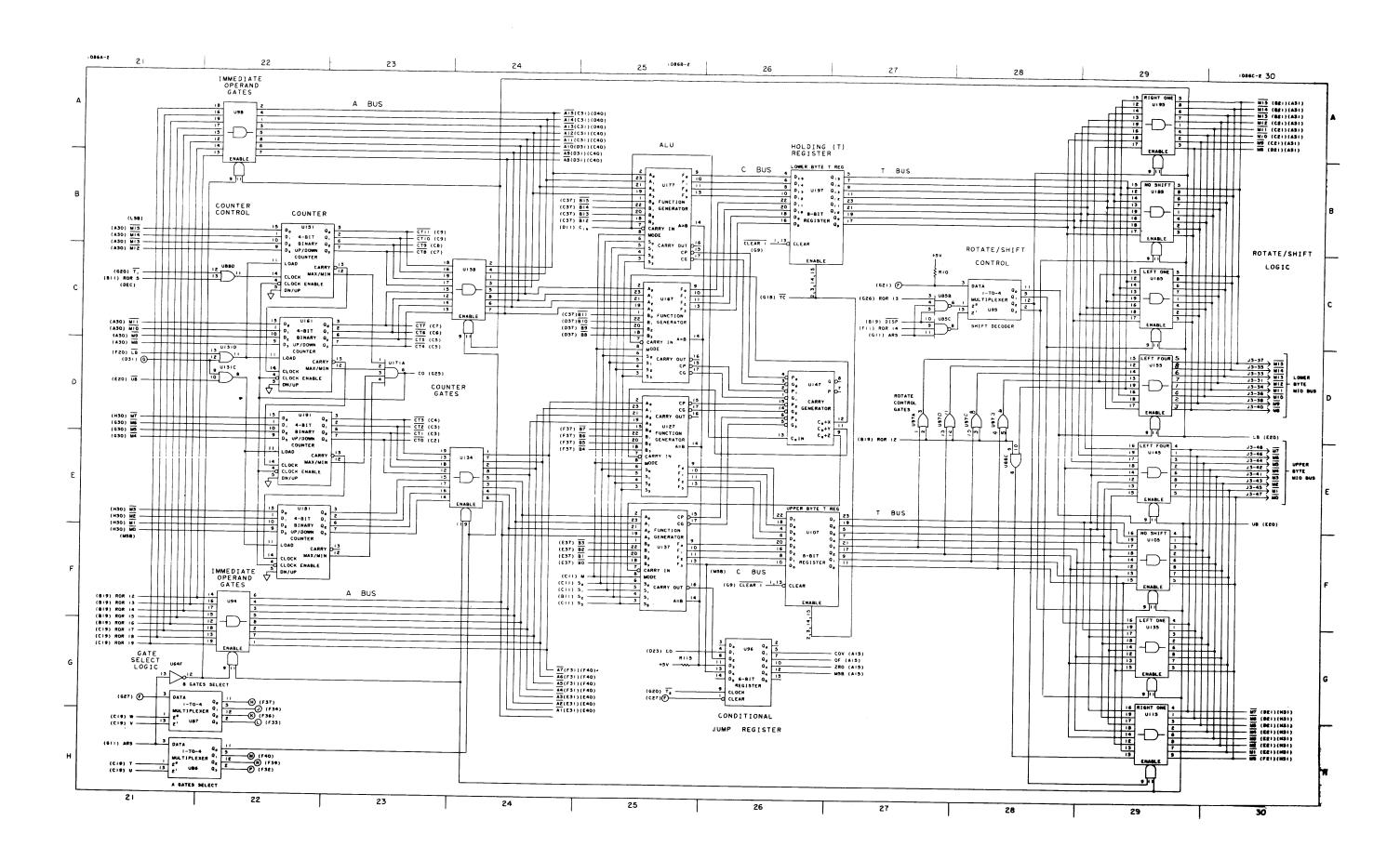


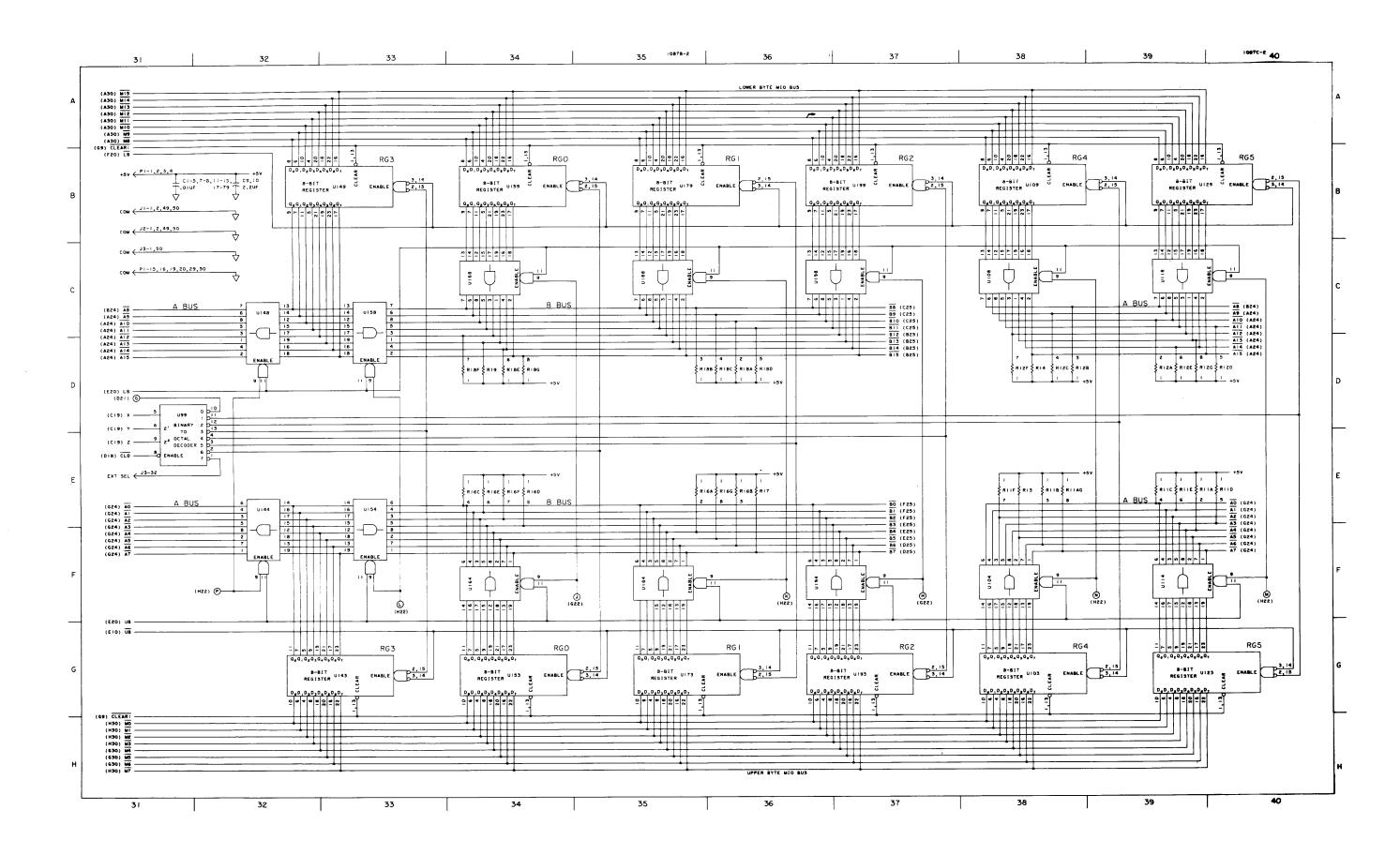


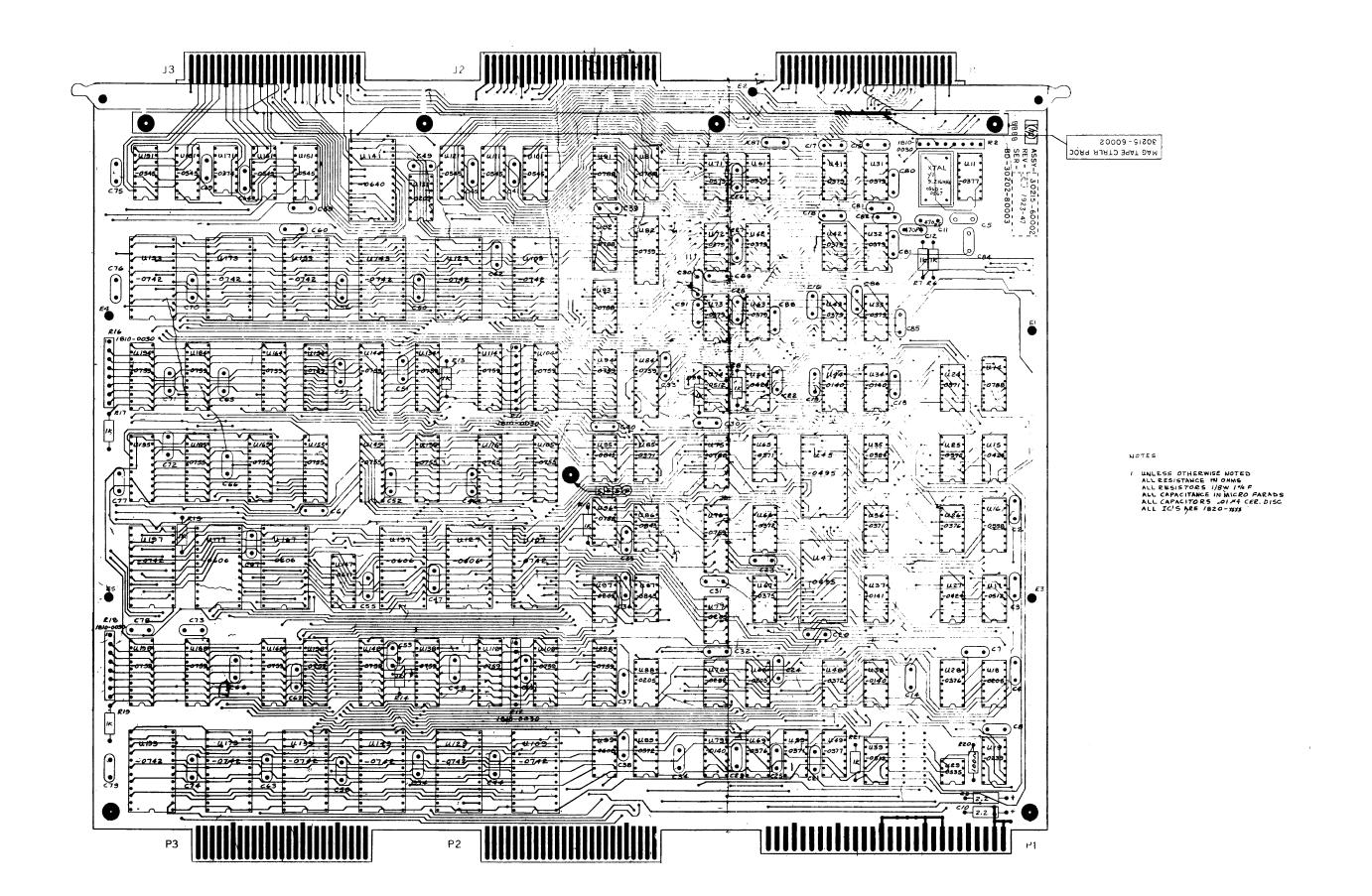


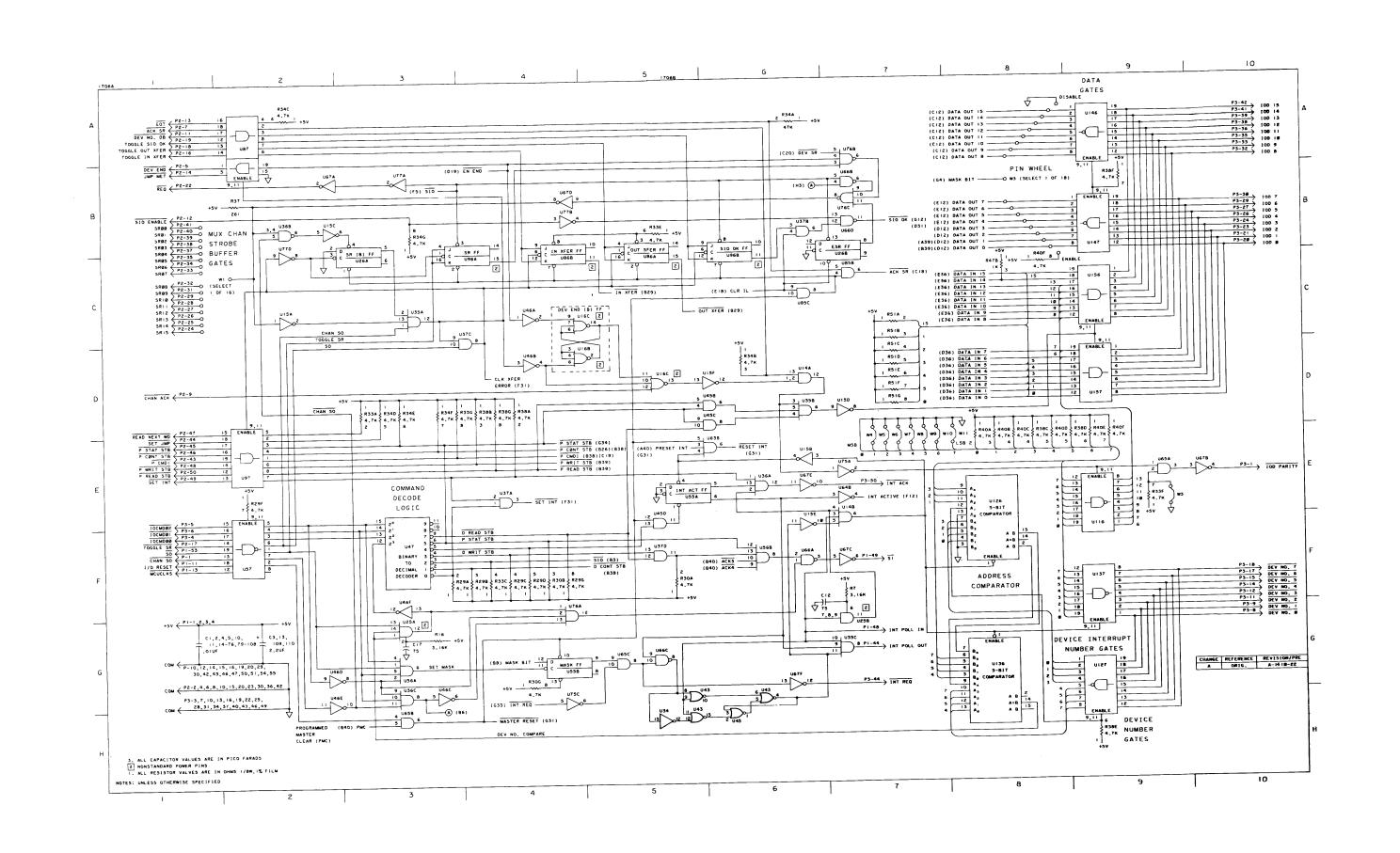


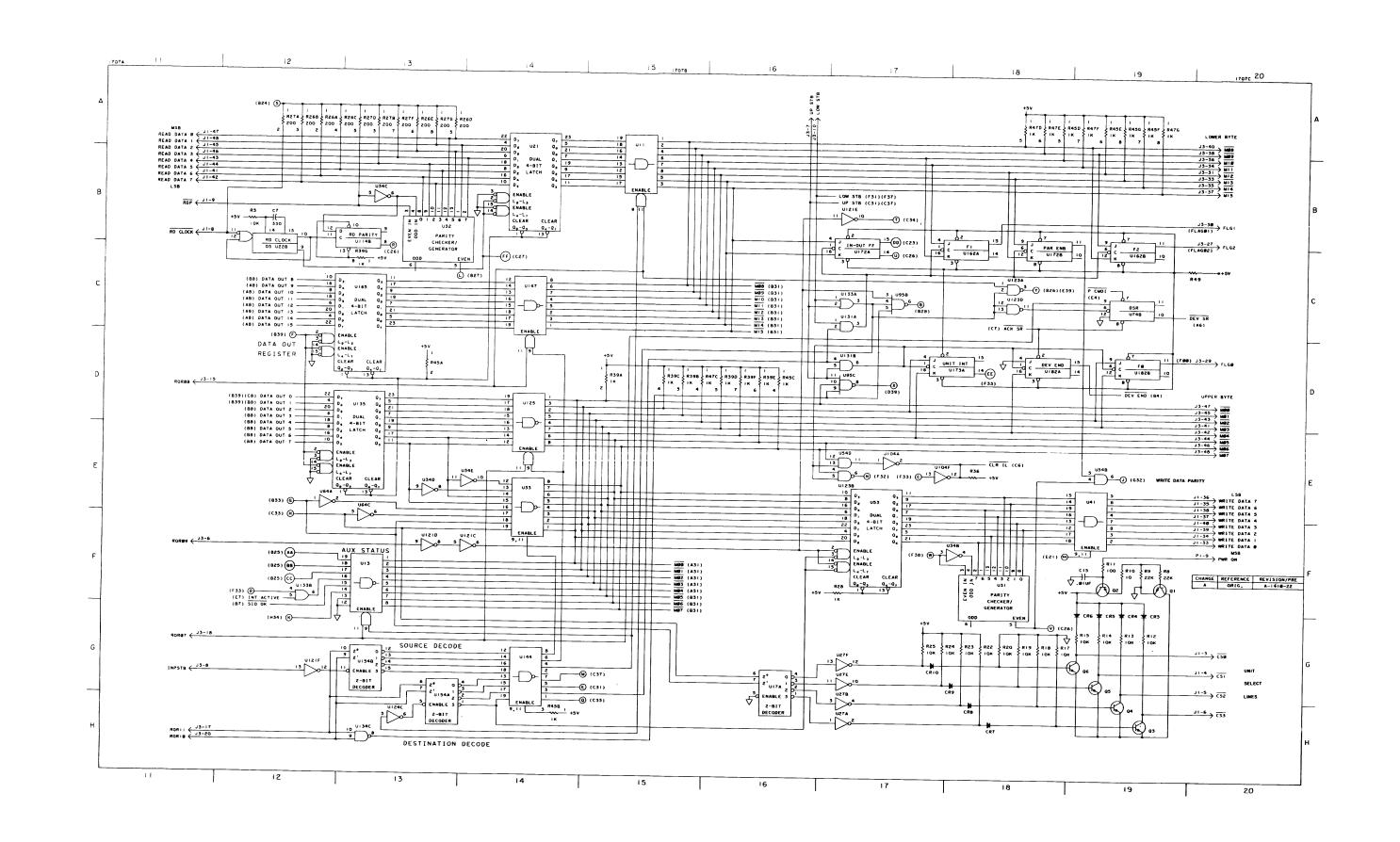


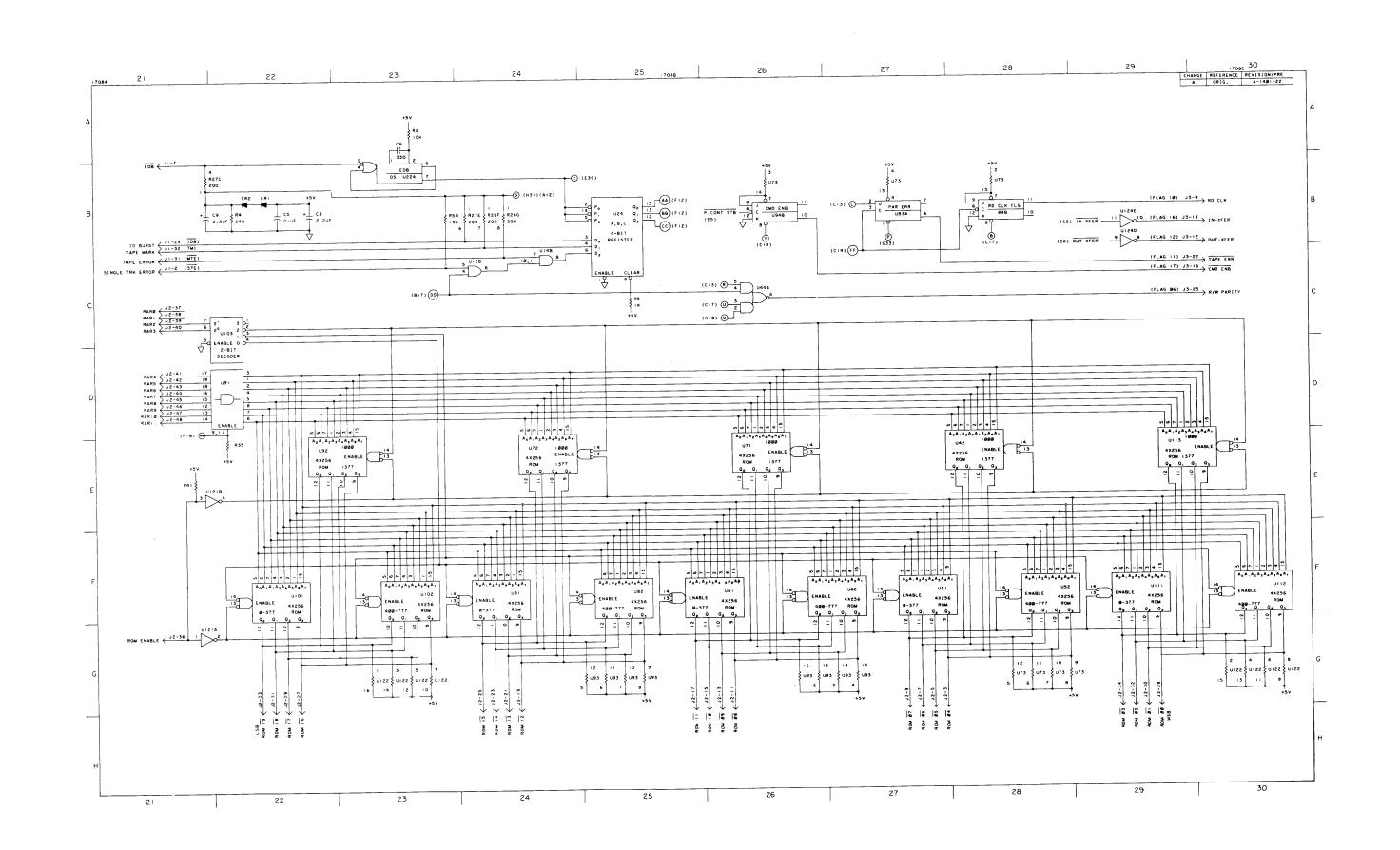


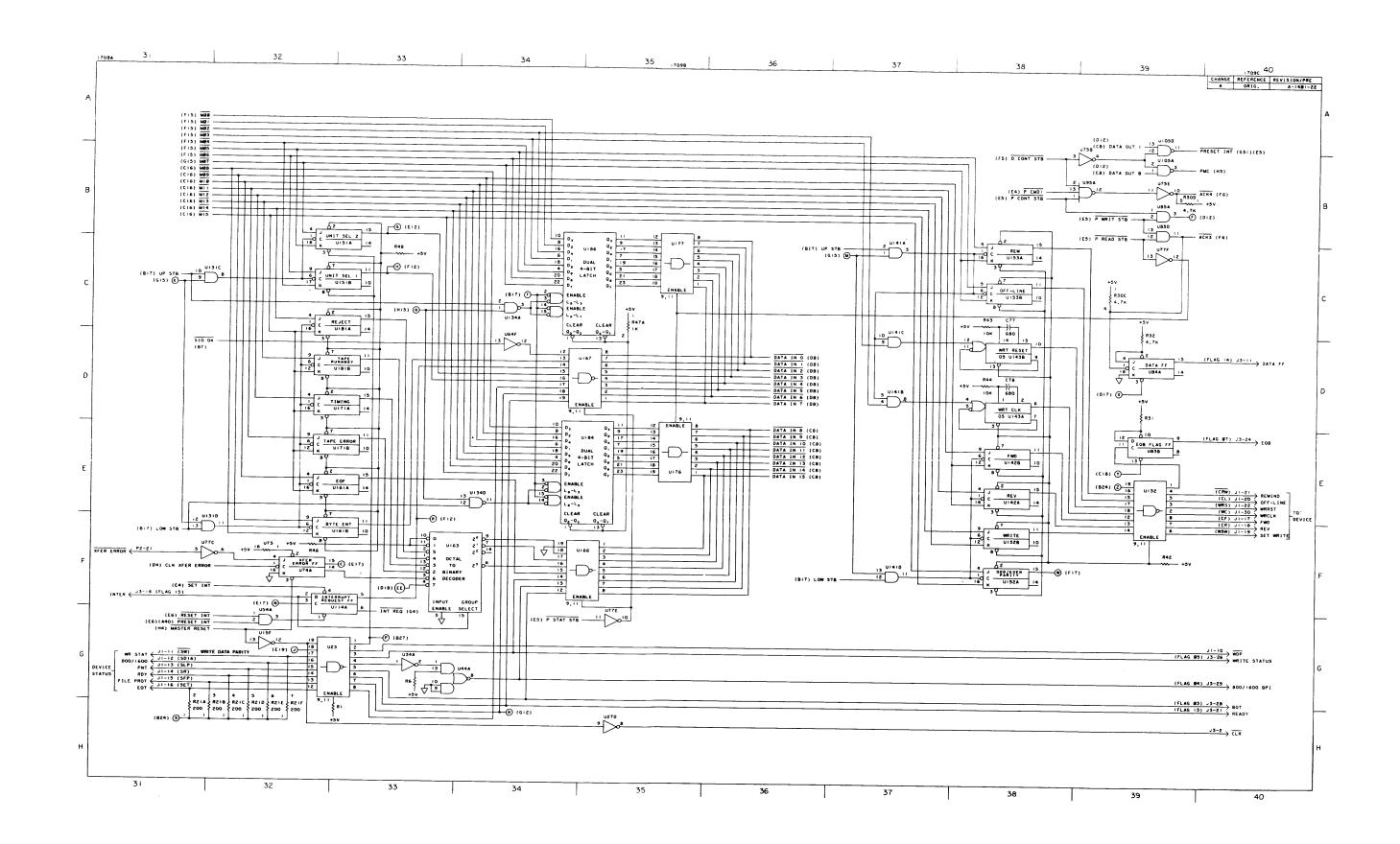




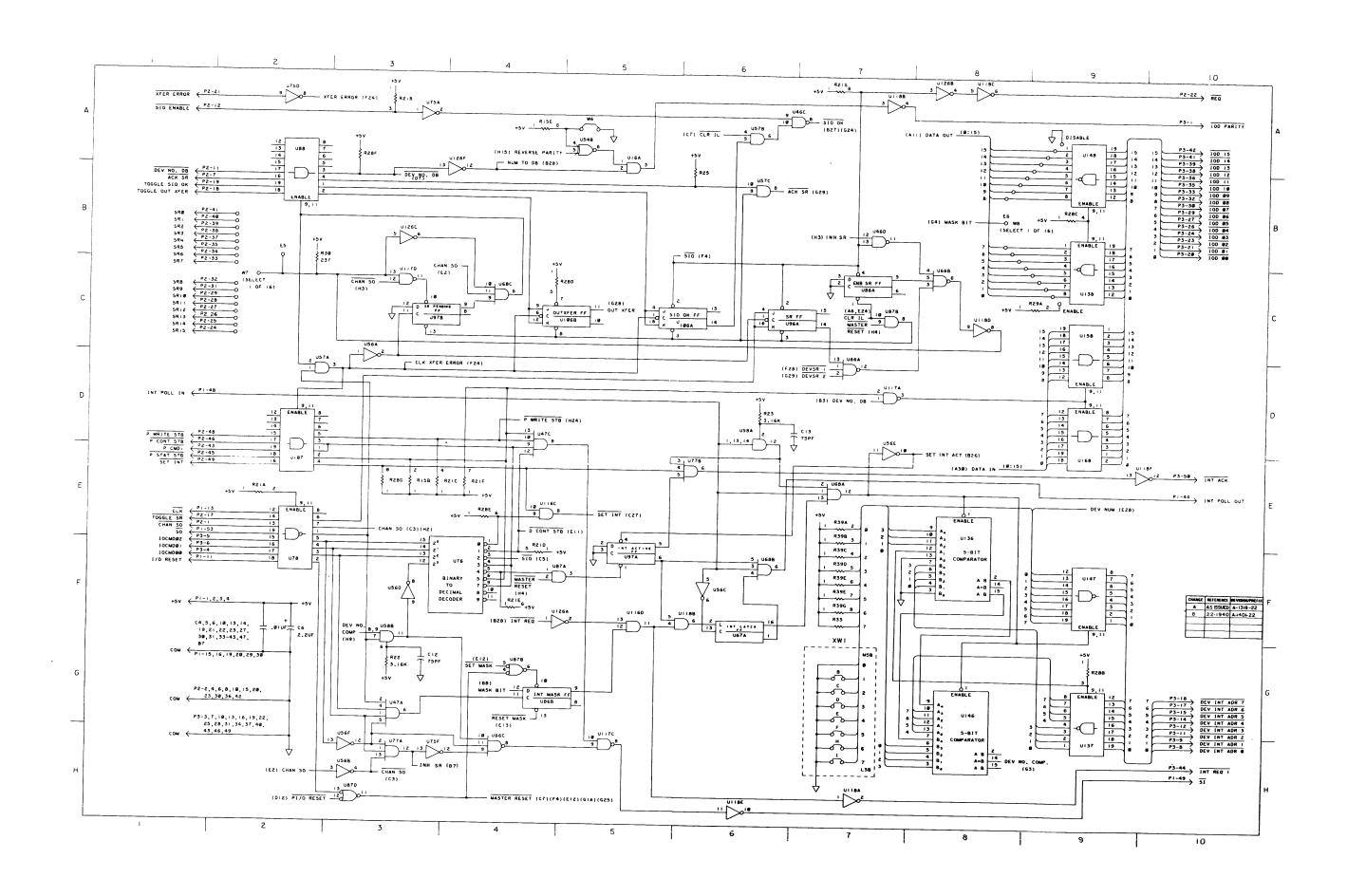




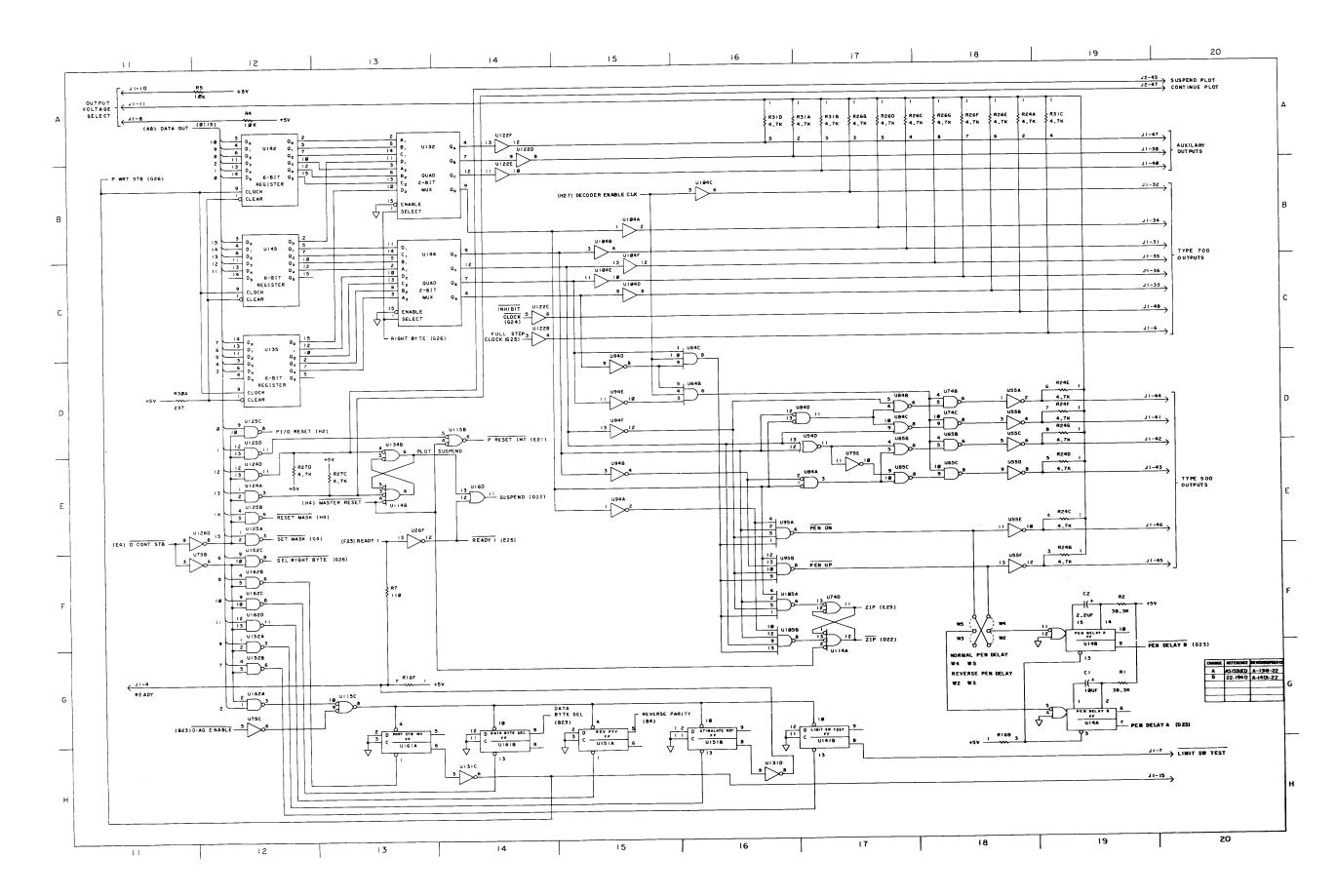


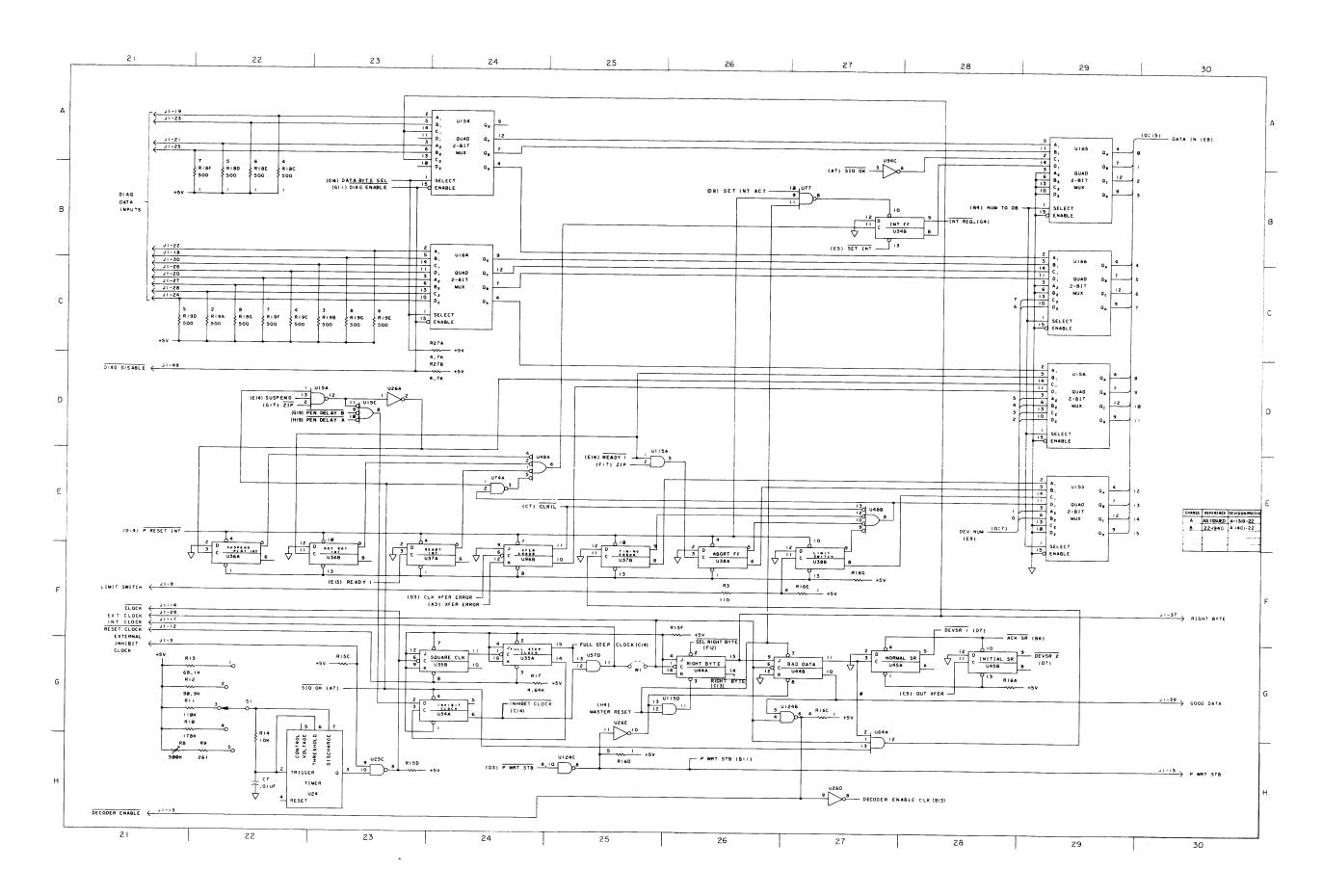


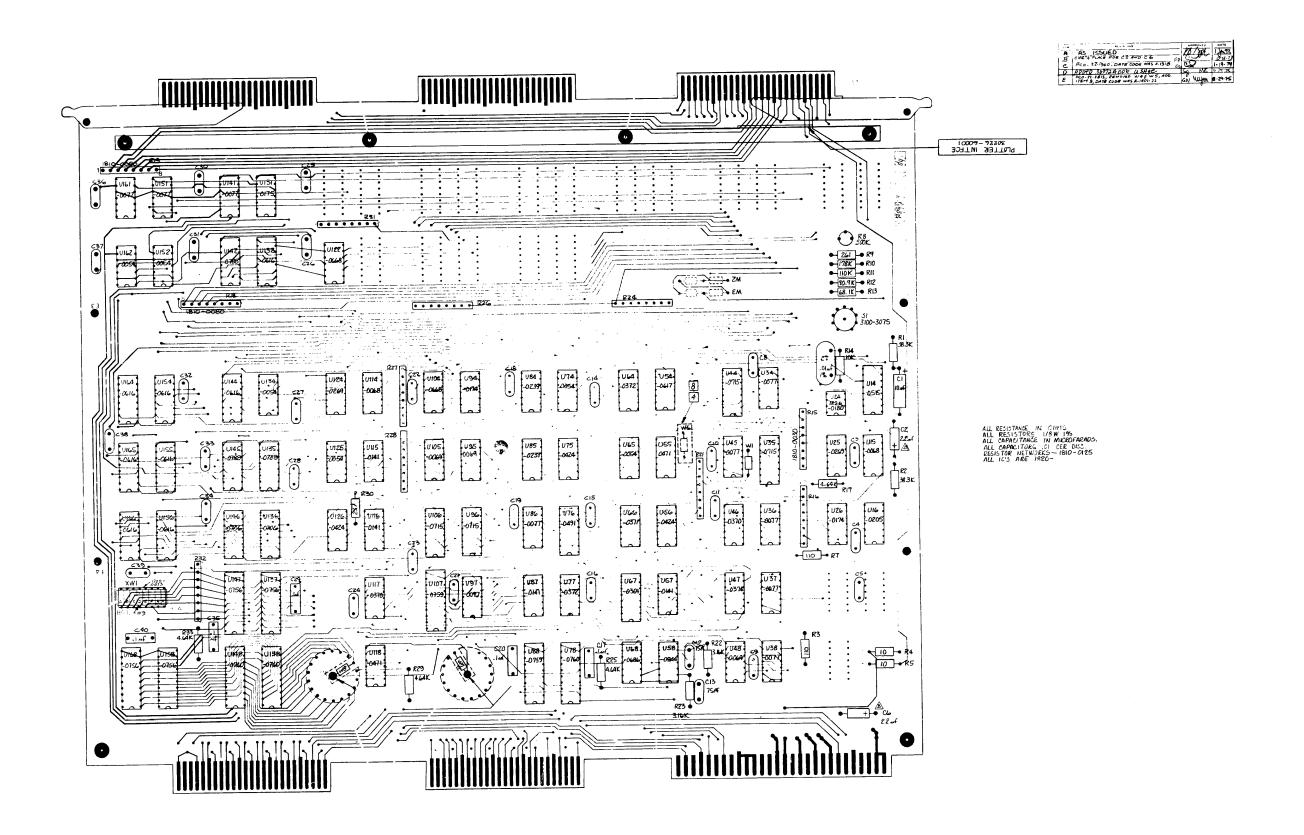


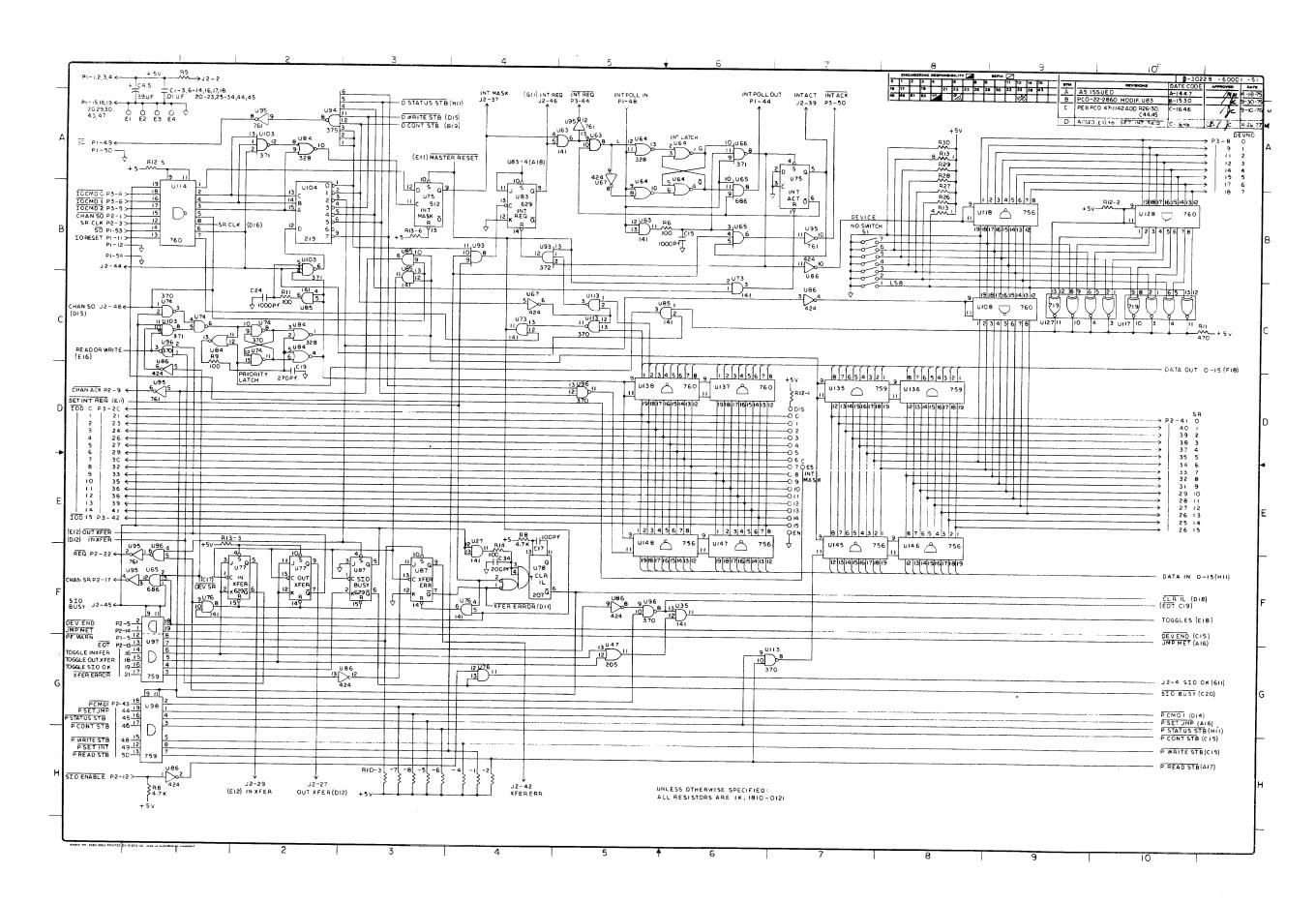


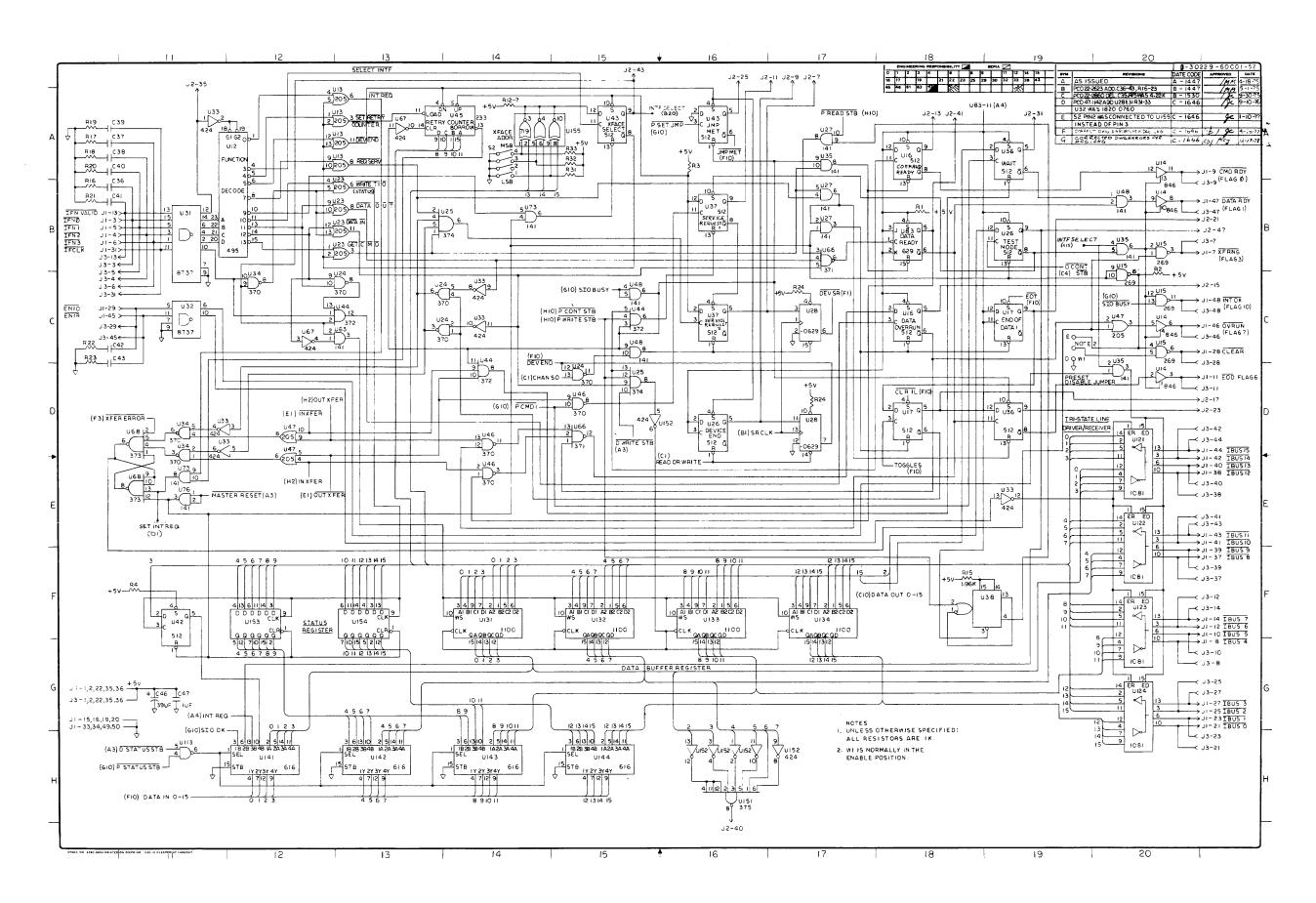
Plotter Interface PCA, 30226-60001, Sheet 1 of 4

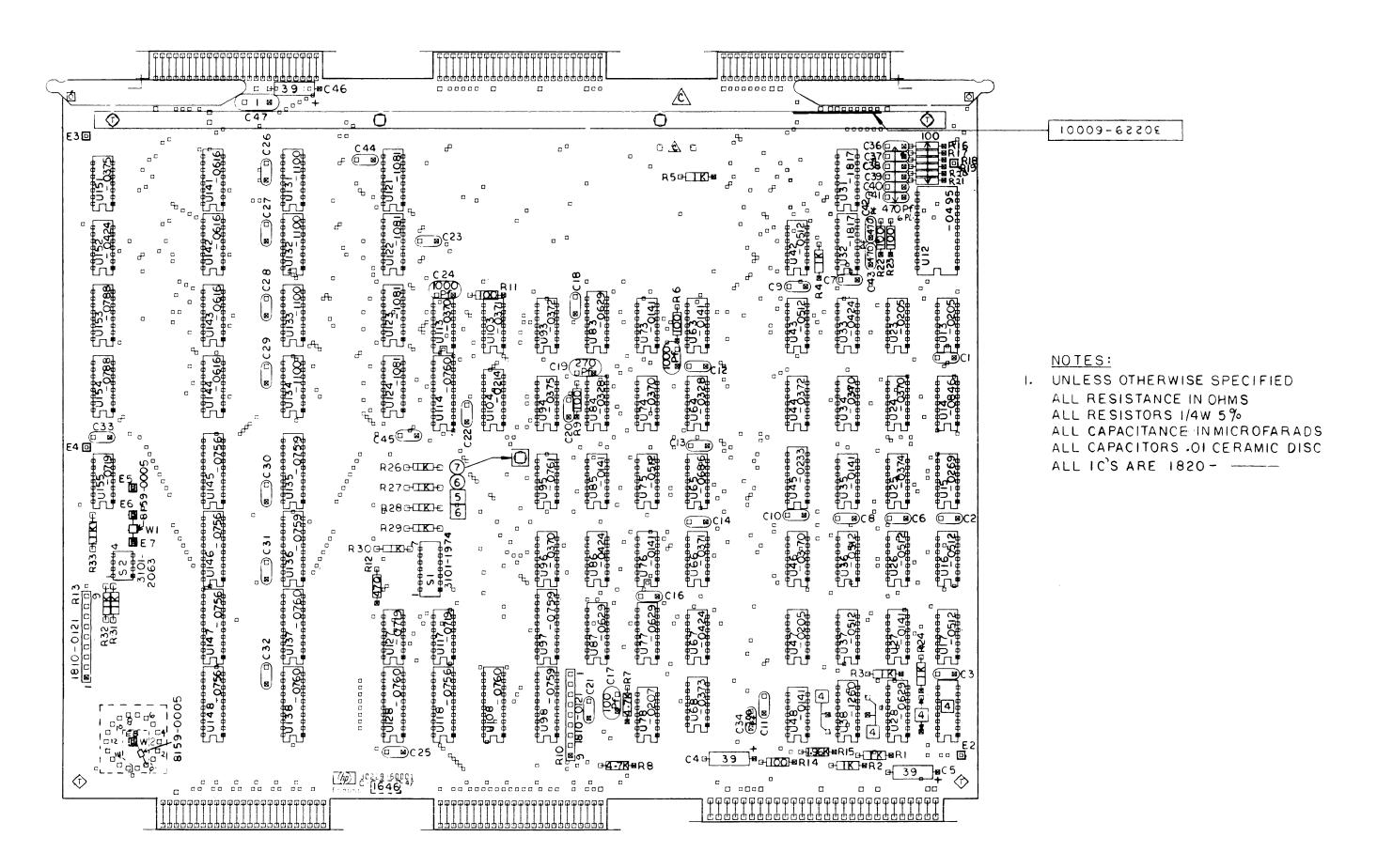


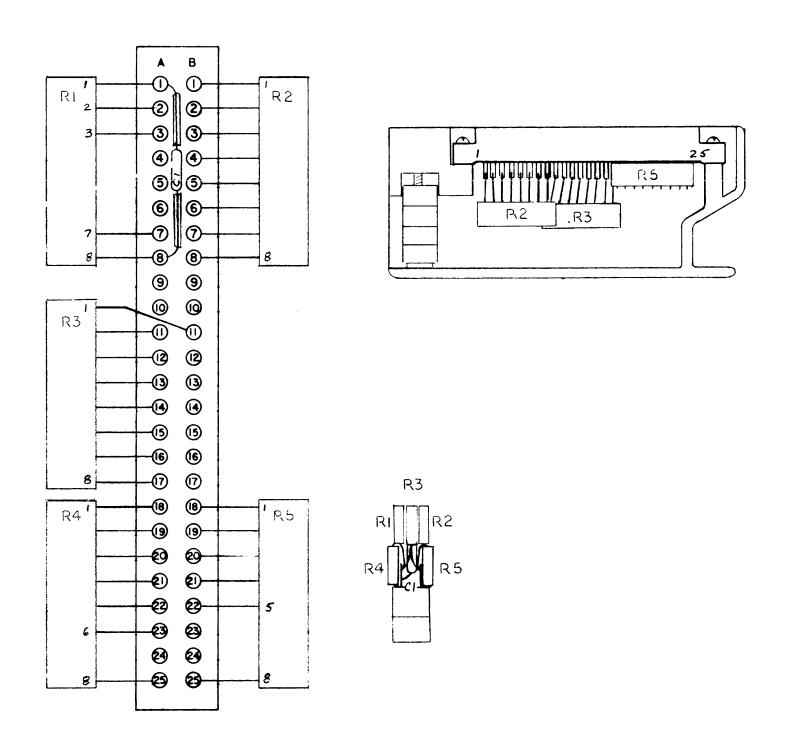


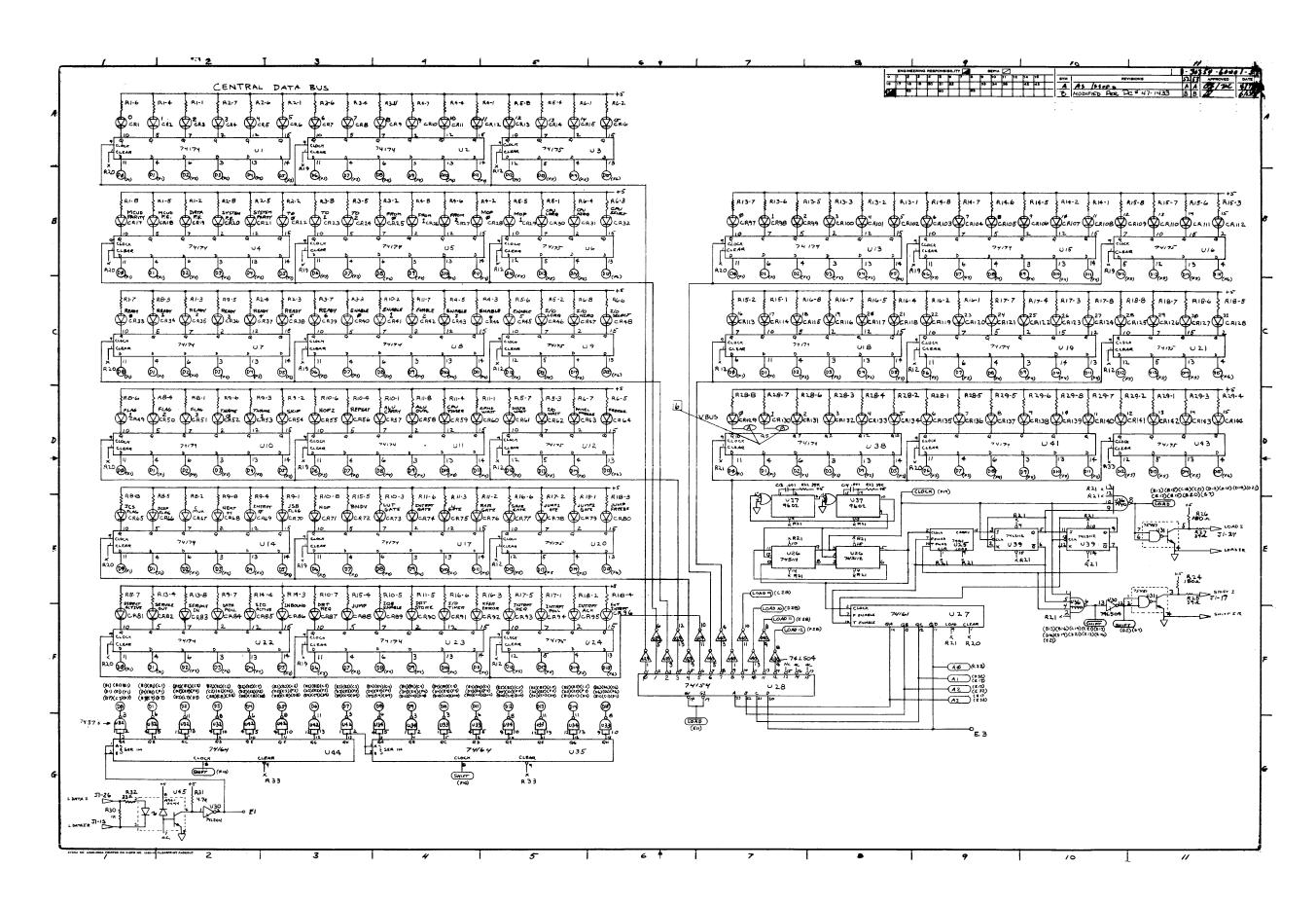


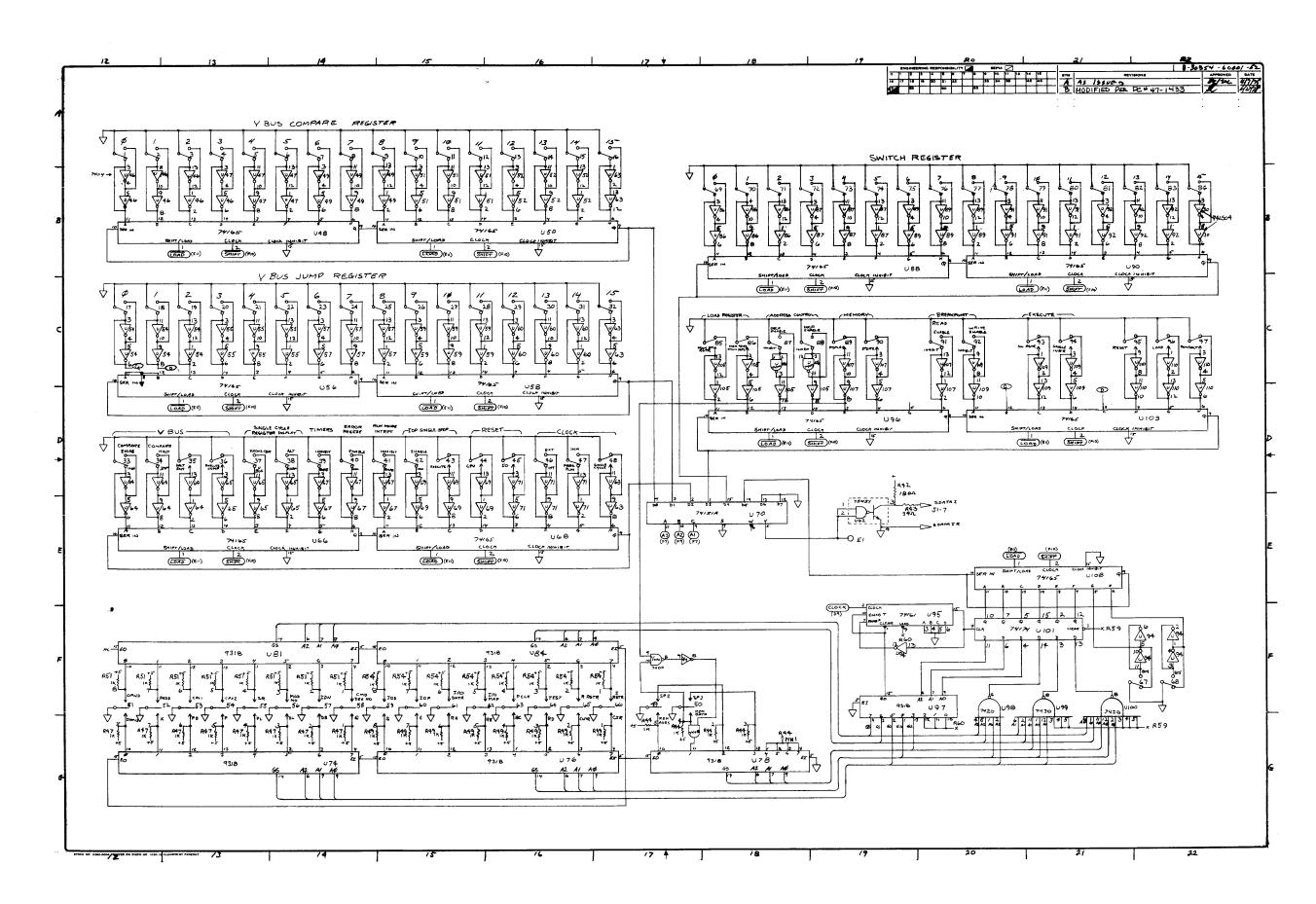


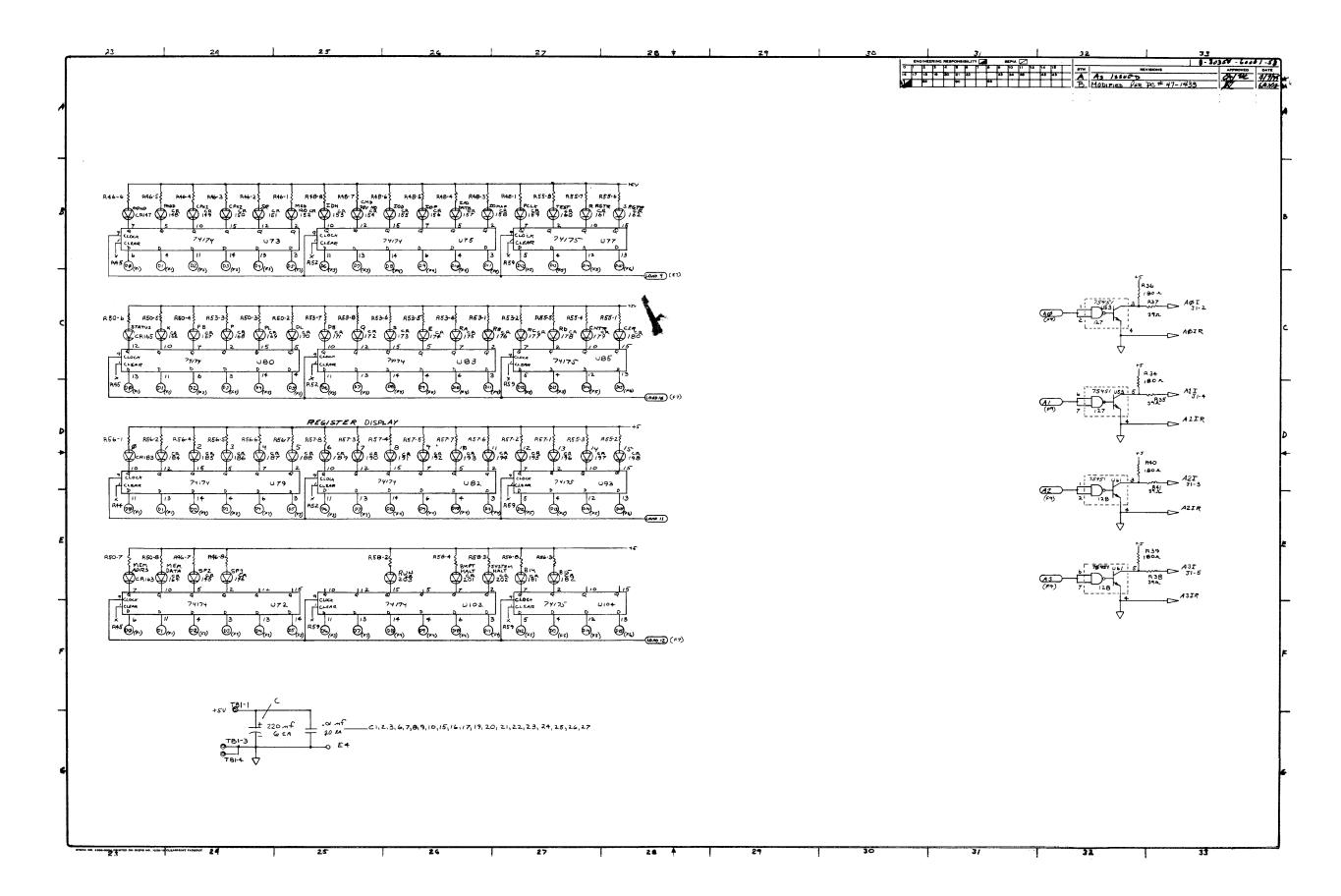


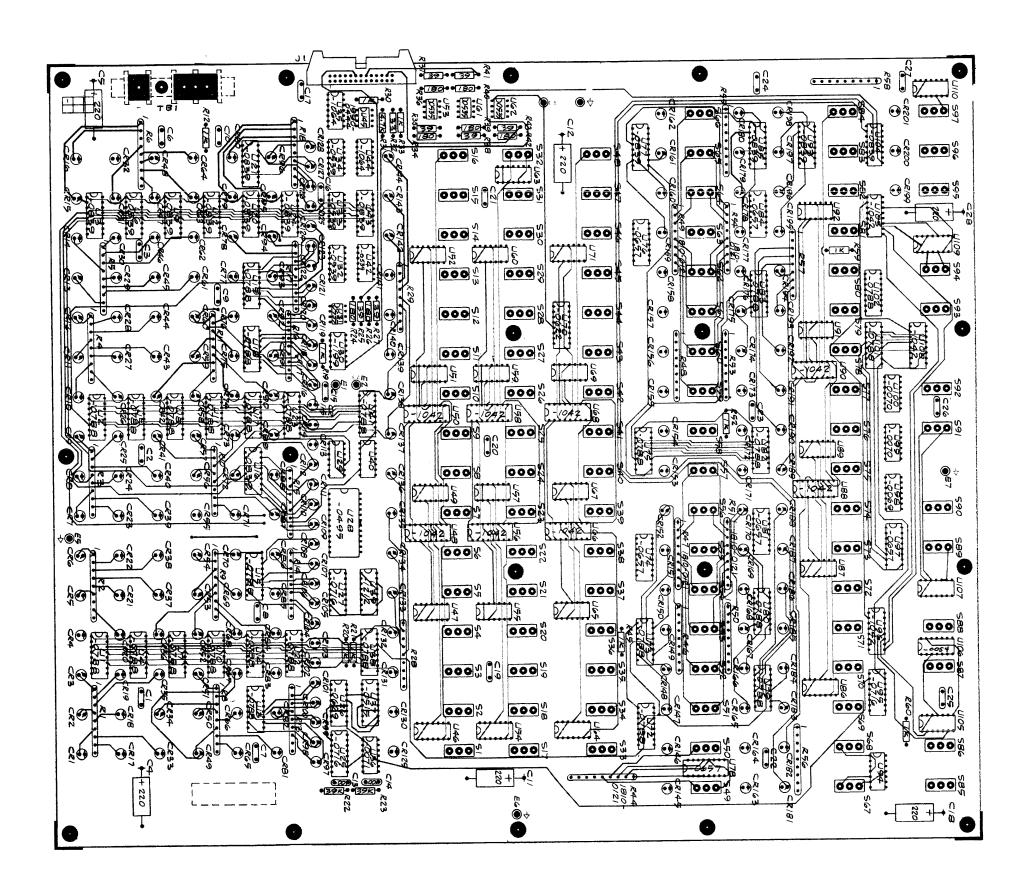






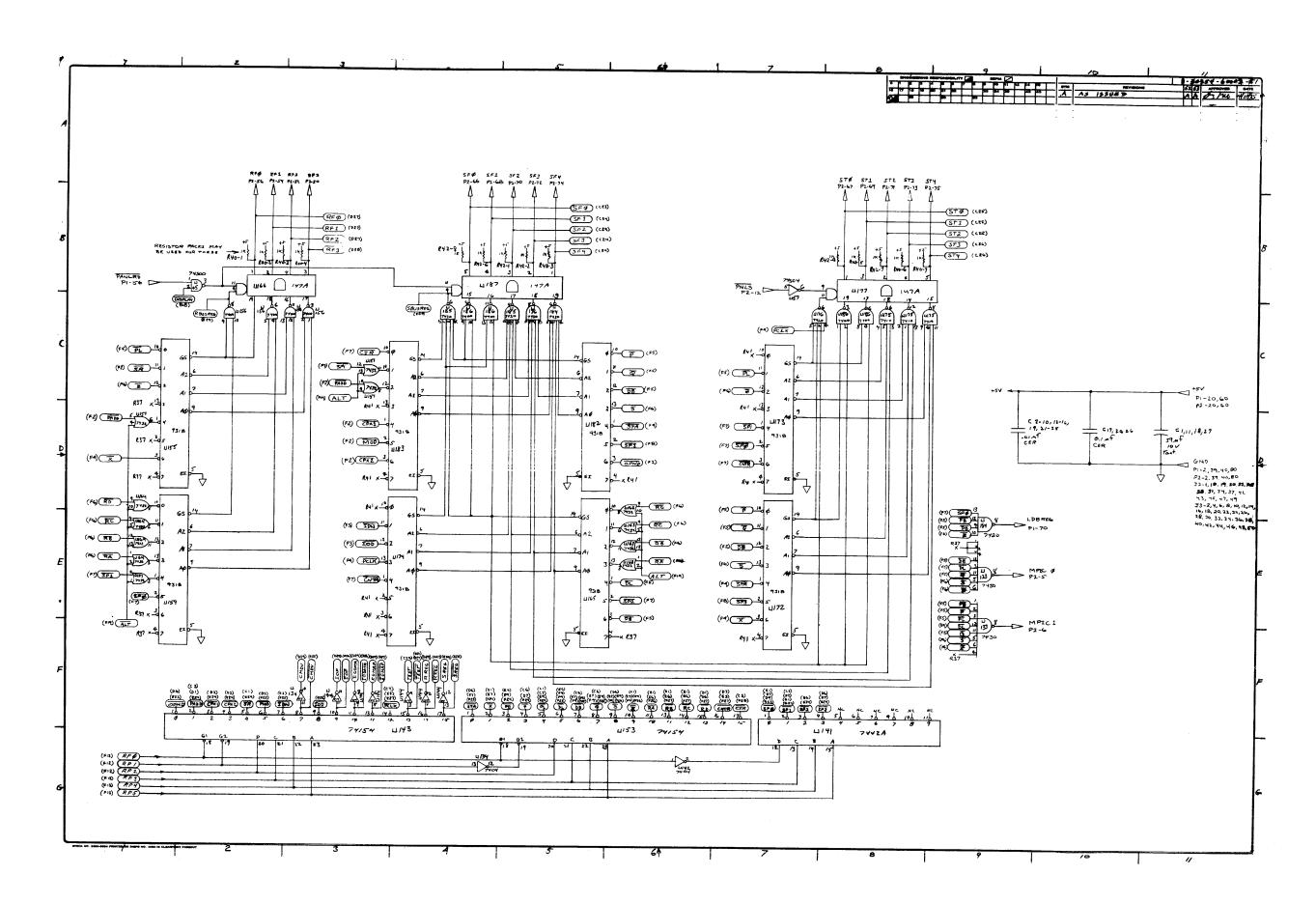


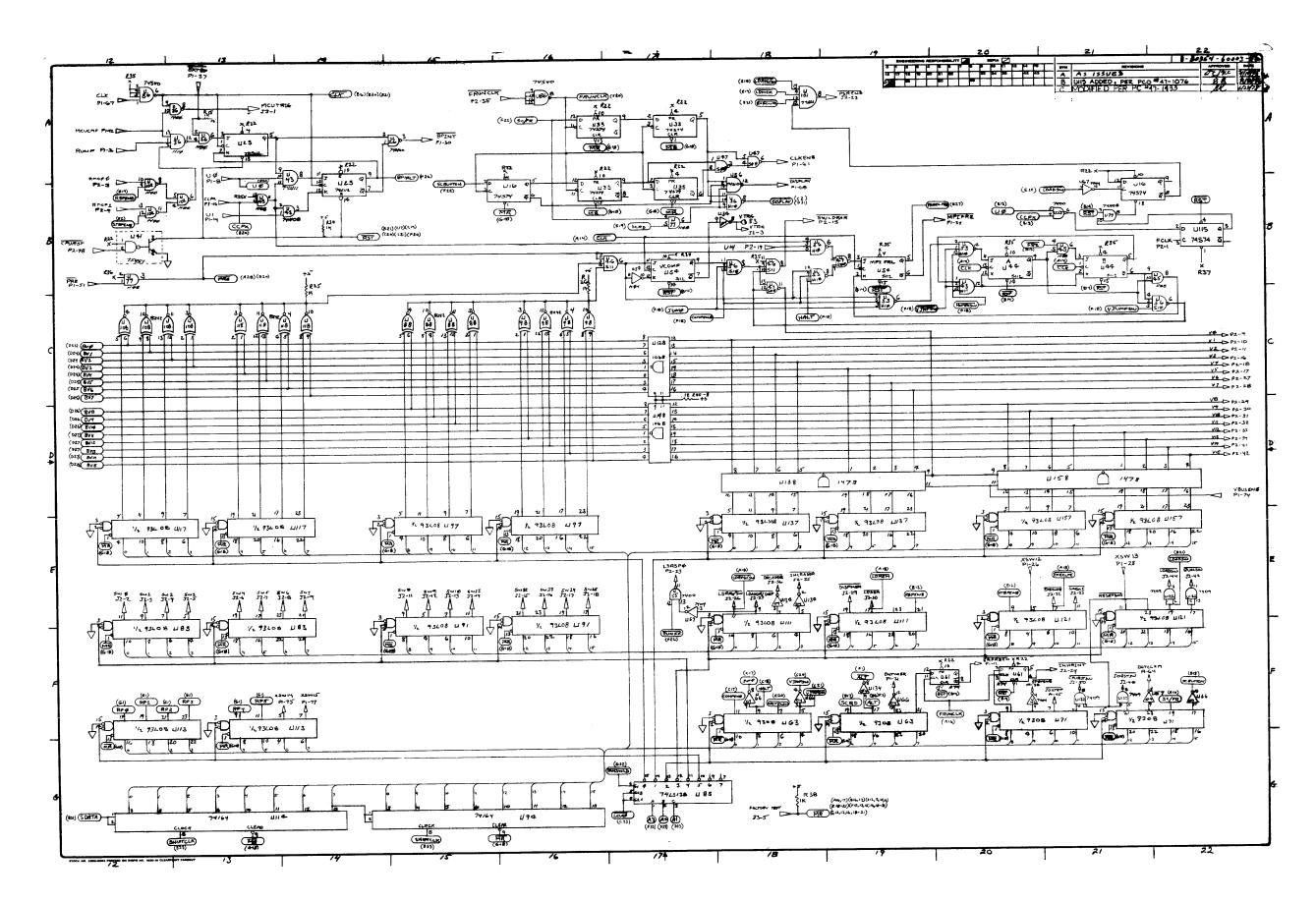


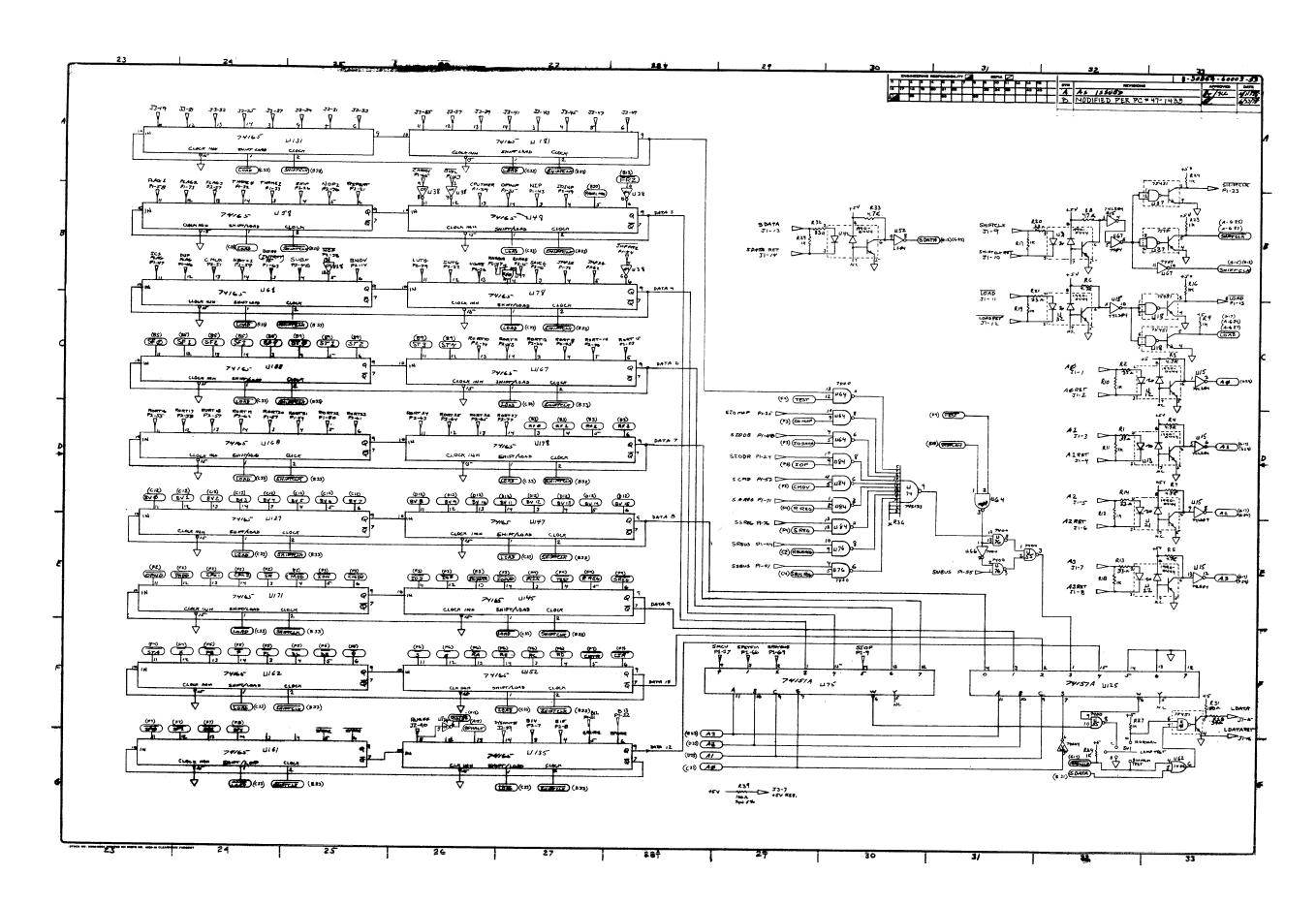


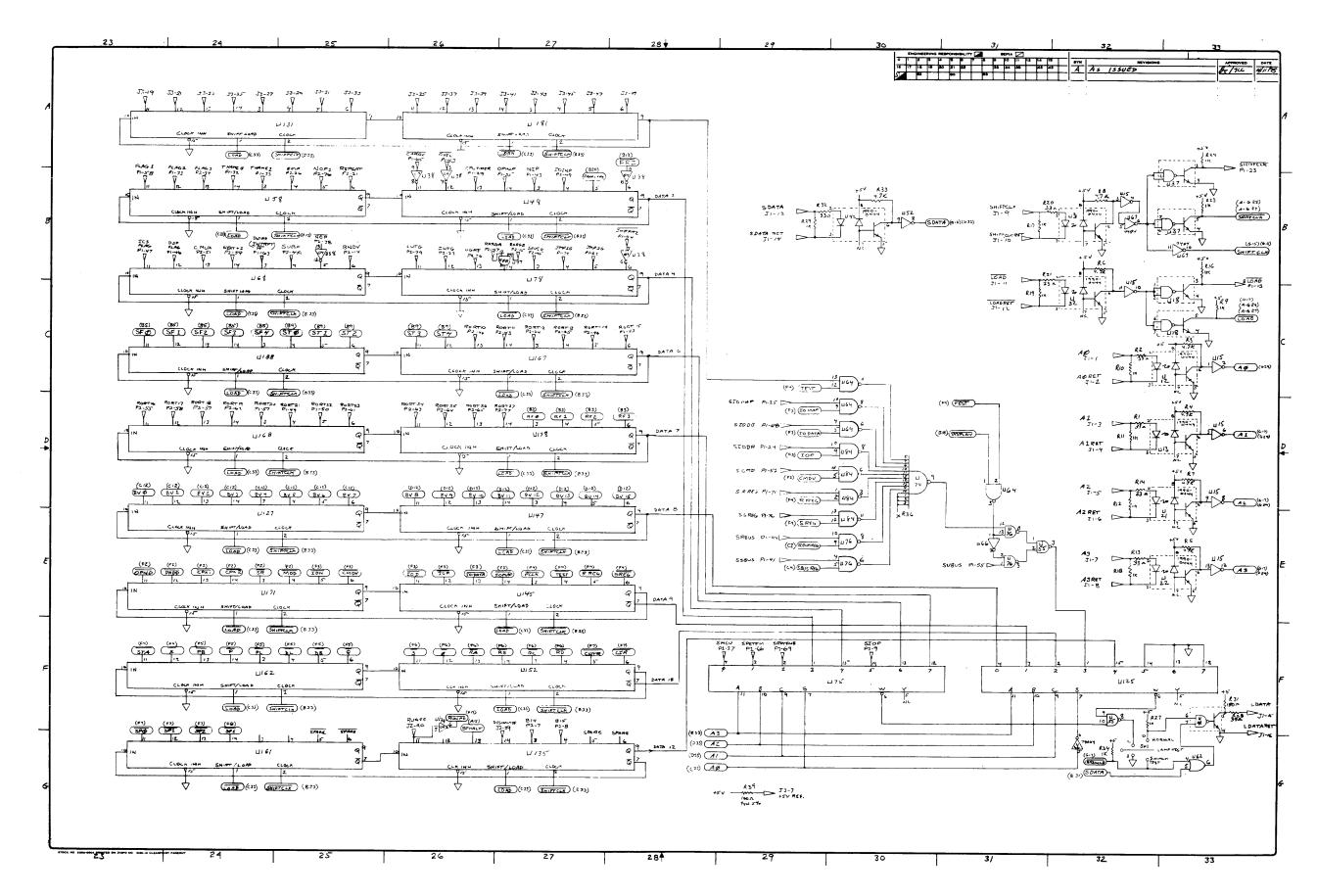
NOTES:

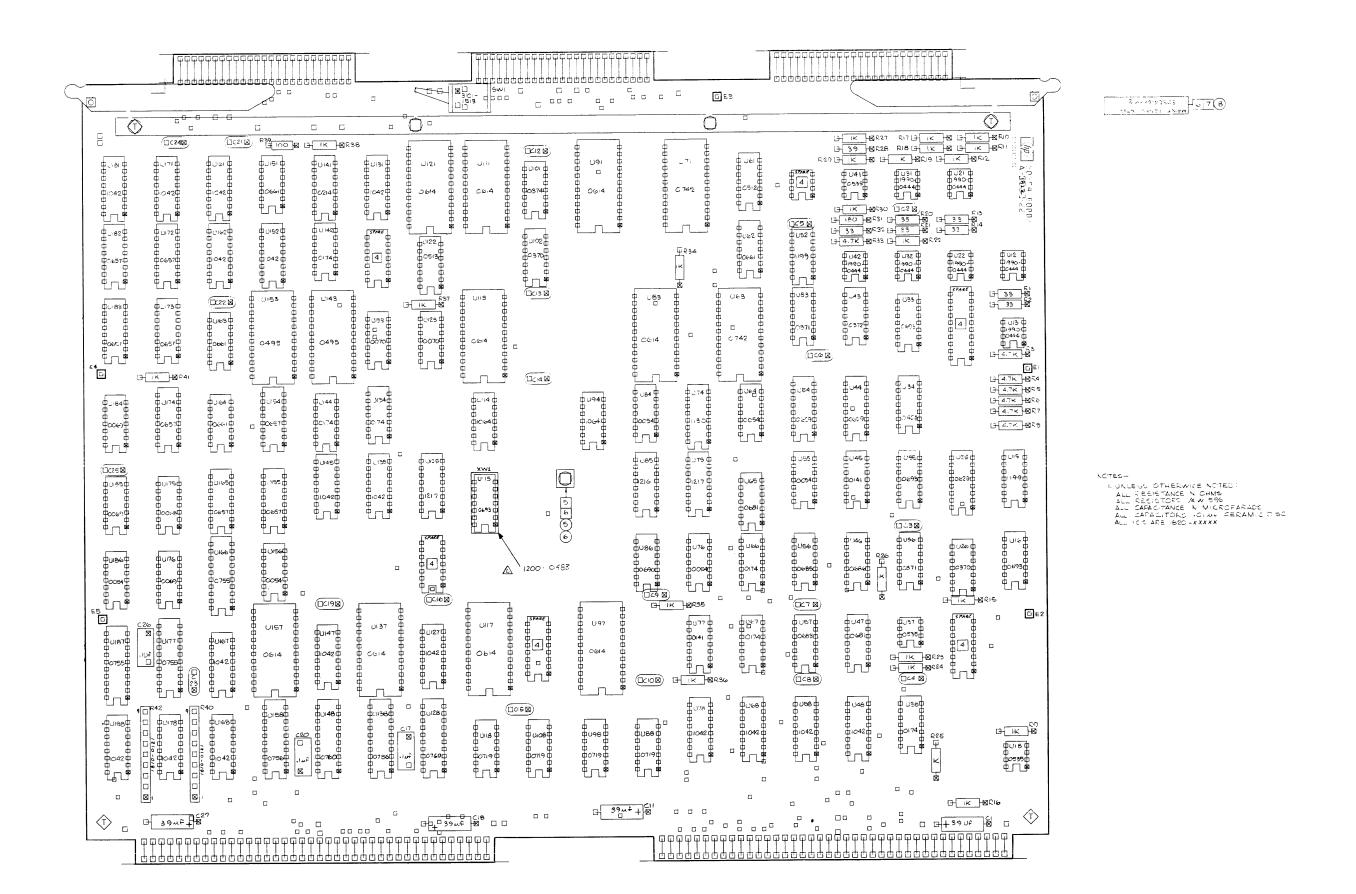
```
1. UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/4W, 9%
ALL CAPACITANCE IN MICROFARADS
ALL CAPACITORS ARE OI CERAMIC DISC
ALL DIODES ARE 1990-0410
ALL RESISTOR NETWORKS ARE 200 SL 1810-0163
ALL I.C.'S ARE 1820-0174
ALL SWITCHES ARE 3101-1941 (CK 7101-7664LE)
549-566 ARE 3101-1948 (CK 7105-CENTER OFF)
539,36,43-45,48,85,86,89,
90,93-97 ARE 3101-1946 (CK 7108-MOMENTARY)
```

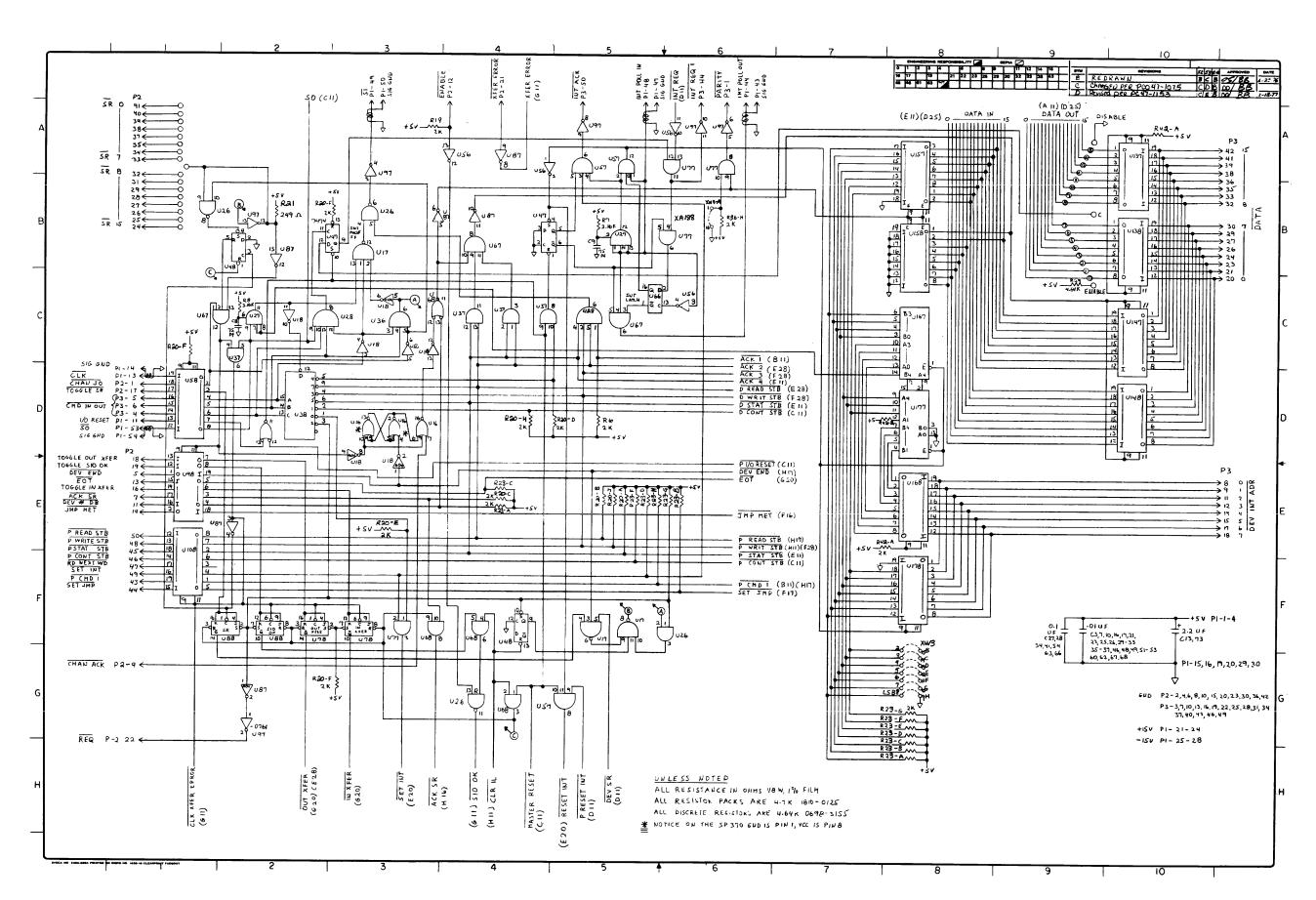


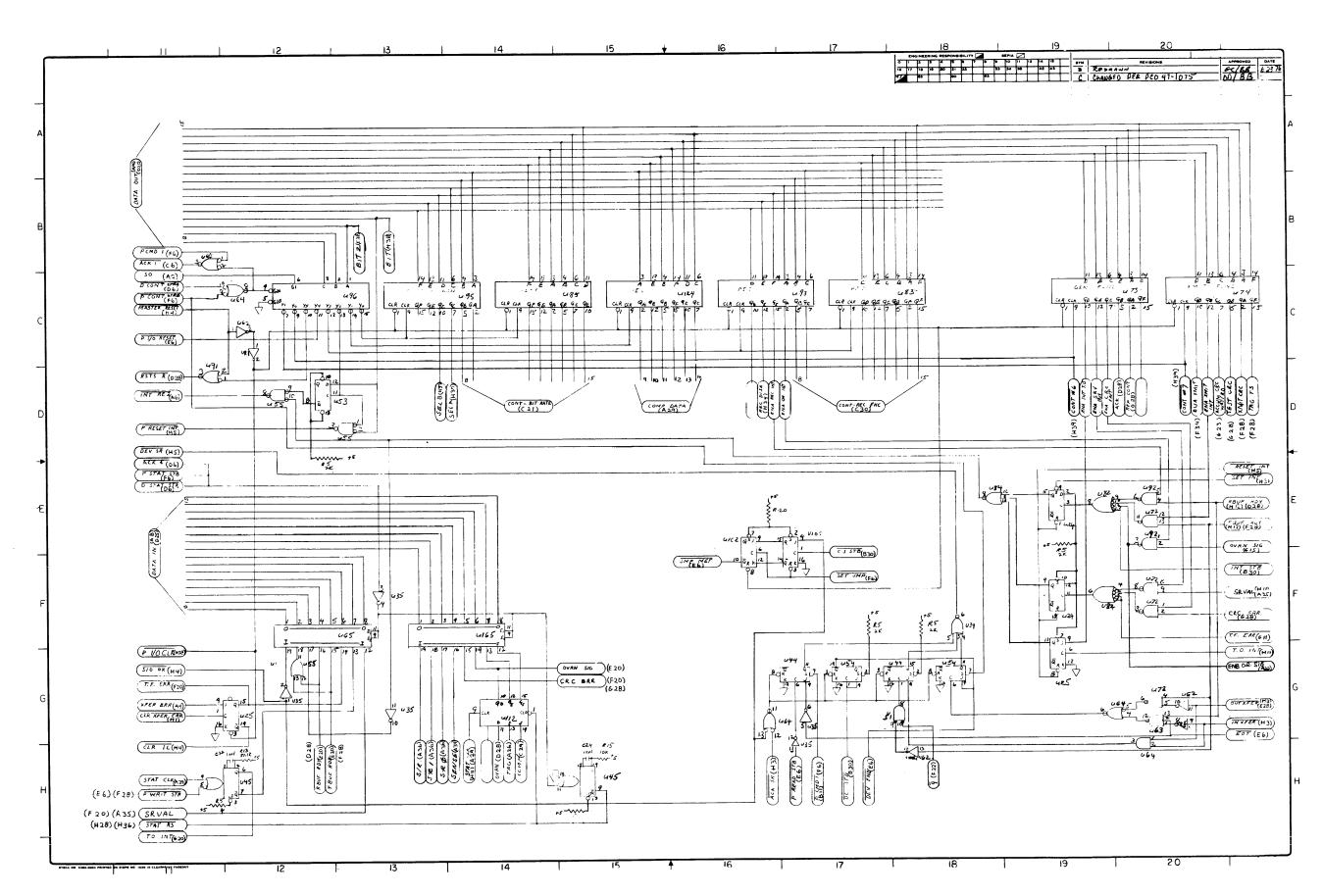




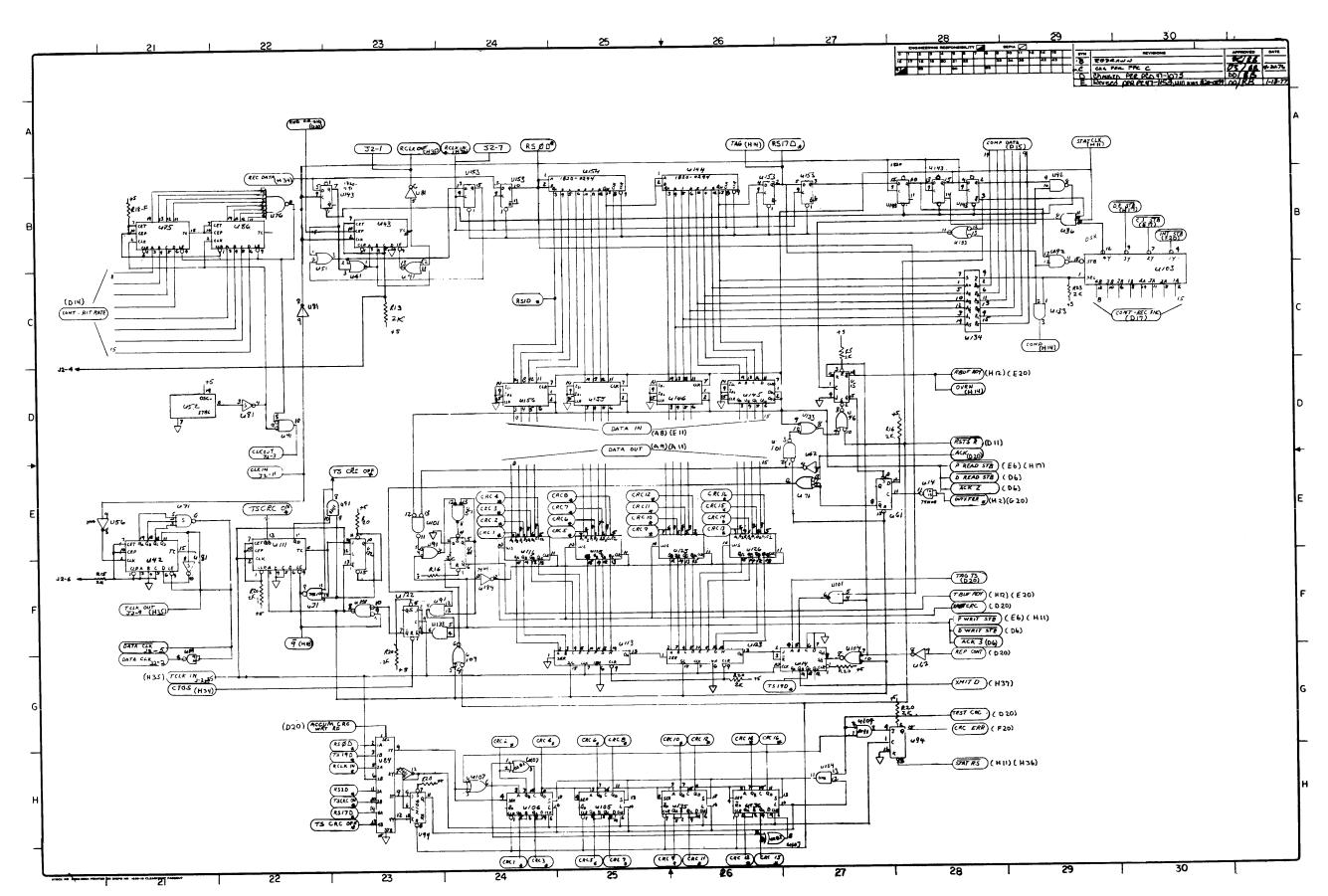




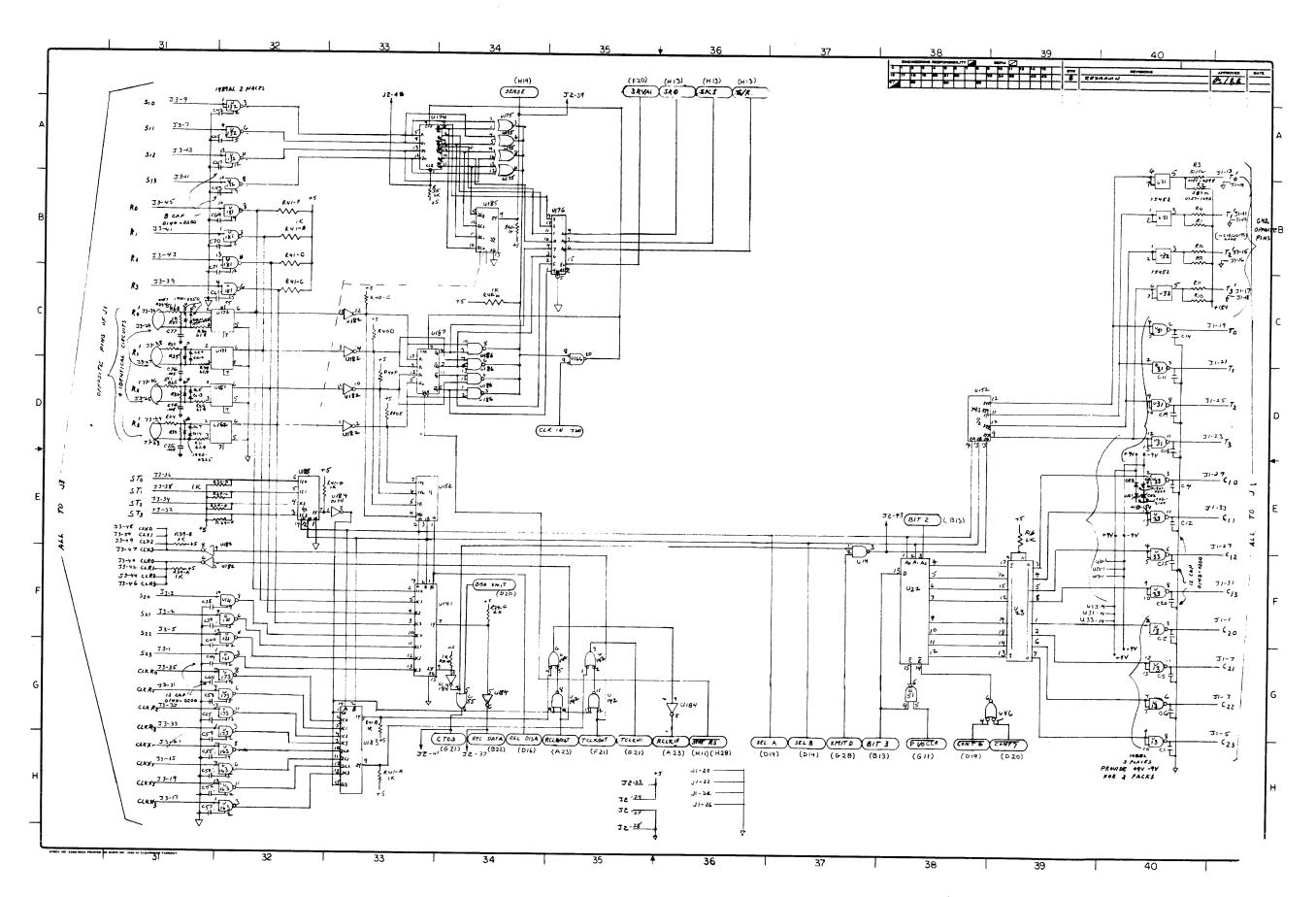


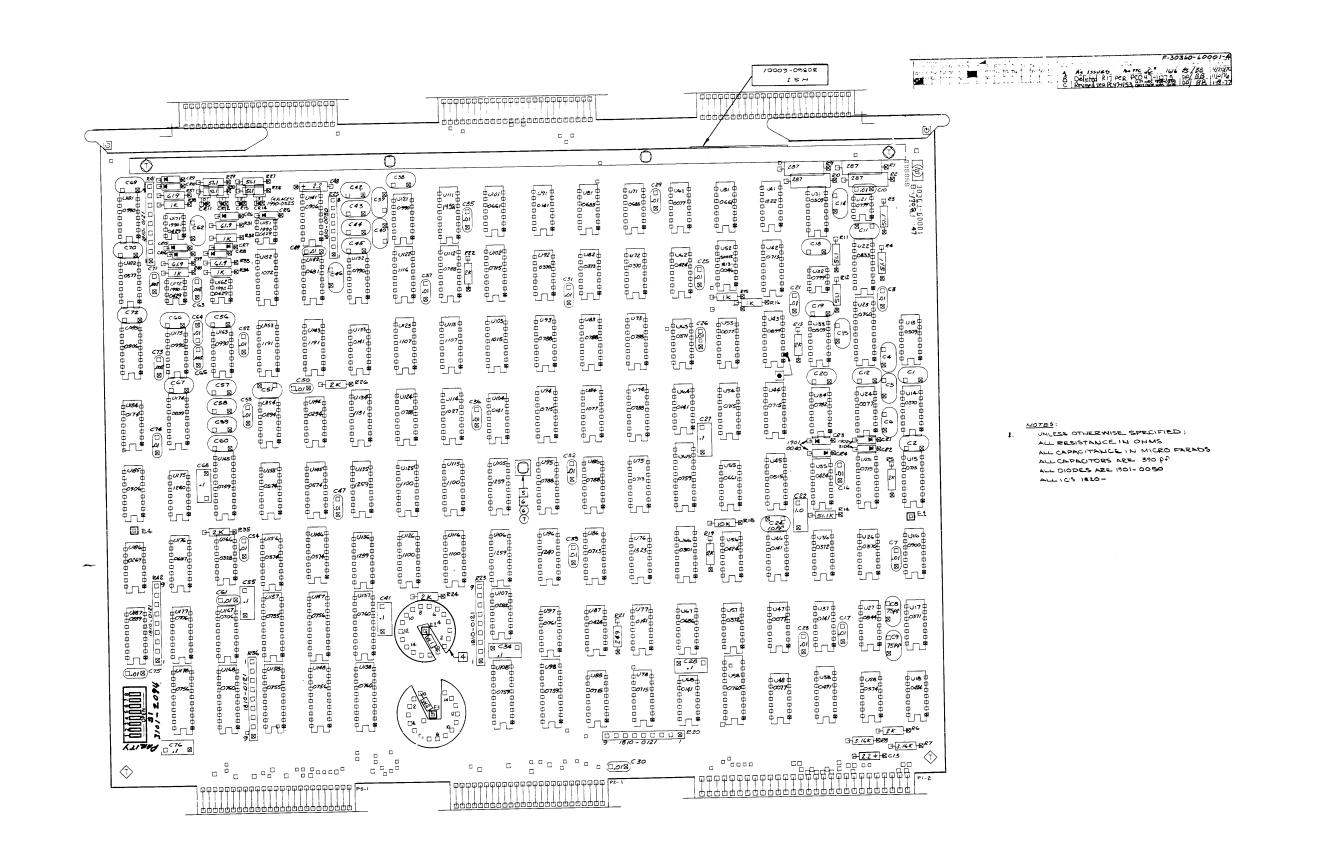


Hardwired Serial Interface, 30360-60001, Sheet 2 of 5



Hardwired Serial Interface, 30360-60001, Sheet 3 of 5

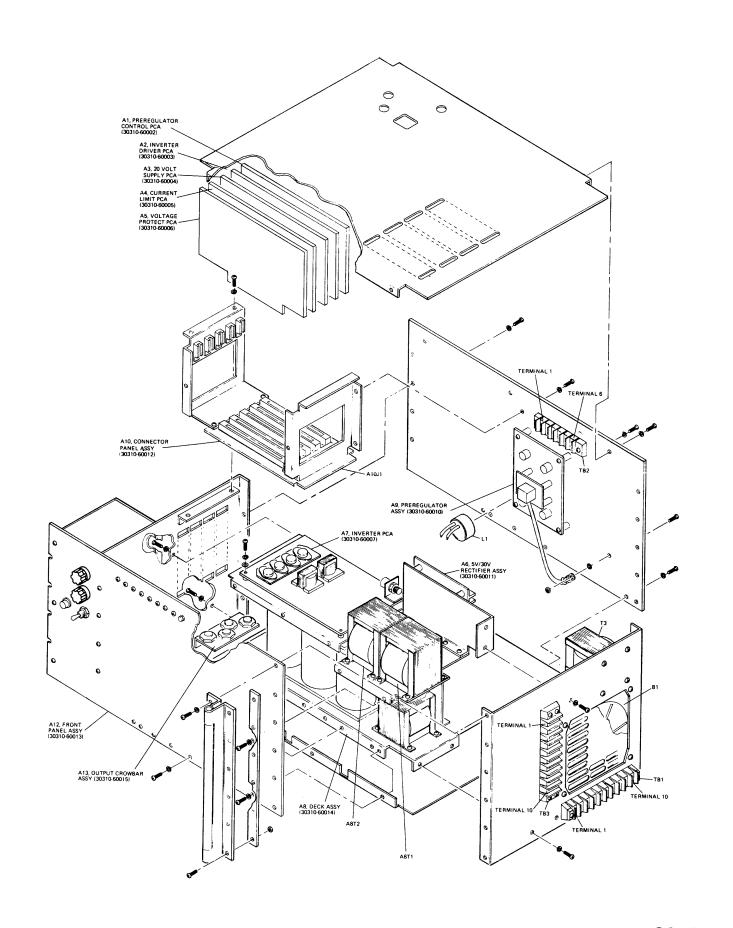


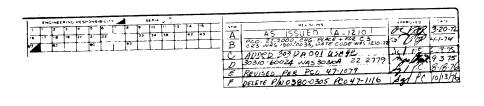


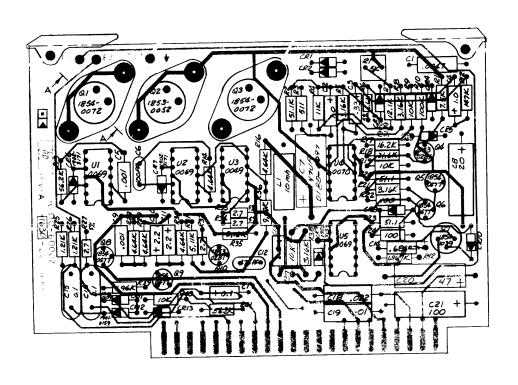
SECTION IV - INDIVIDUAL POWER SUPPLIES

CONTENTS

NUMBER	DESCRIPTION
(None)32421A30	3104 Power Supply, Exploded View
20210 60002	Al, Preregulator
00010 00002	A A A A A A A A A A A A A A A A A A A
20210 60004	a a a a a a a a a a a a a a a a a a a
00010 00005	Current Dimit
00010 60006	AJ, VOITAGE ITOUCO
20210 60011	
20210 60007	A A A A A A A A A A A A A A A A A A A
20210 60014	Assembly
30310-60014	Than t Danel of 30310A Supply
30310-60010	A13. Output Crowbar
(37 · · · ·)	Landa POWEL Dubbiy, 0001011
00011 (0000)	SUSTIA POWEL BUDDLY, MOUNCE FOR
00011 00009	
20211 60005	
00010 00001	303 ZA POWEL Supply, Assembly
30312-60002	
00010	32435APower Control Display PCA
30135-60016	DC Power Control PCA
30135-60017	







NOTES !

I. UNLESS OTHERWISE SPECIFIED

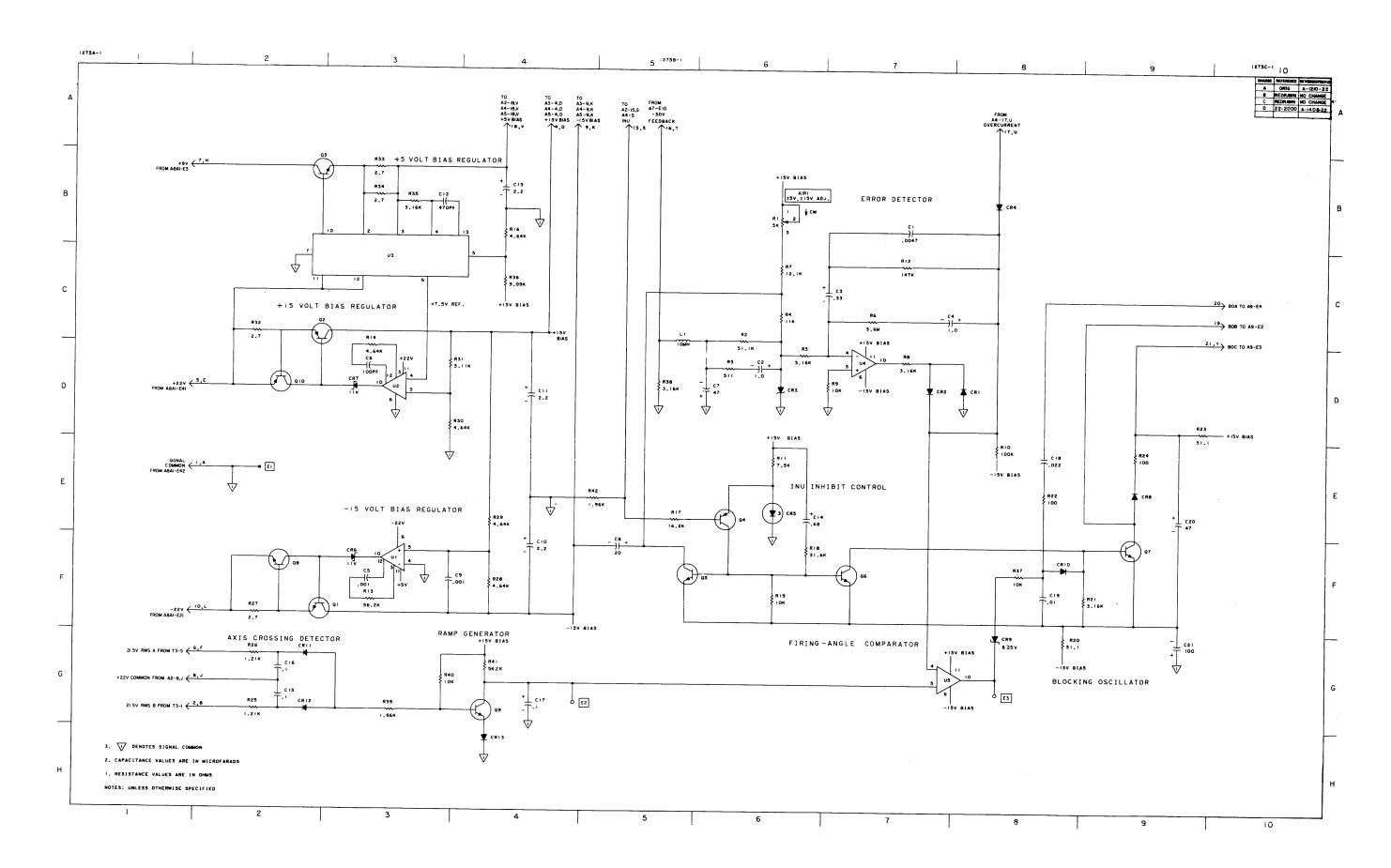
ALL RESISTANCE IN OHMS

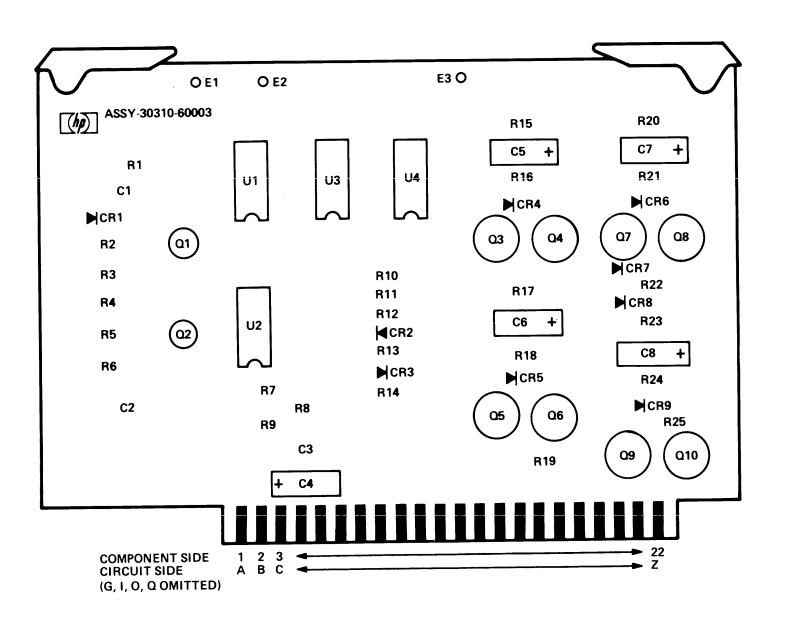
ALL RESISTOR 1/4W, ± 1%

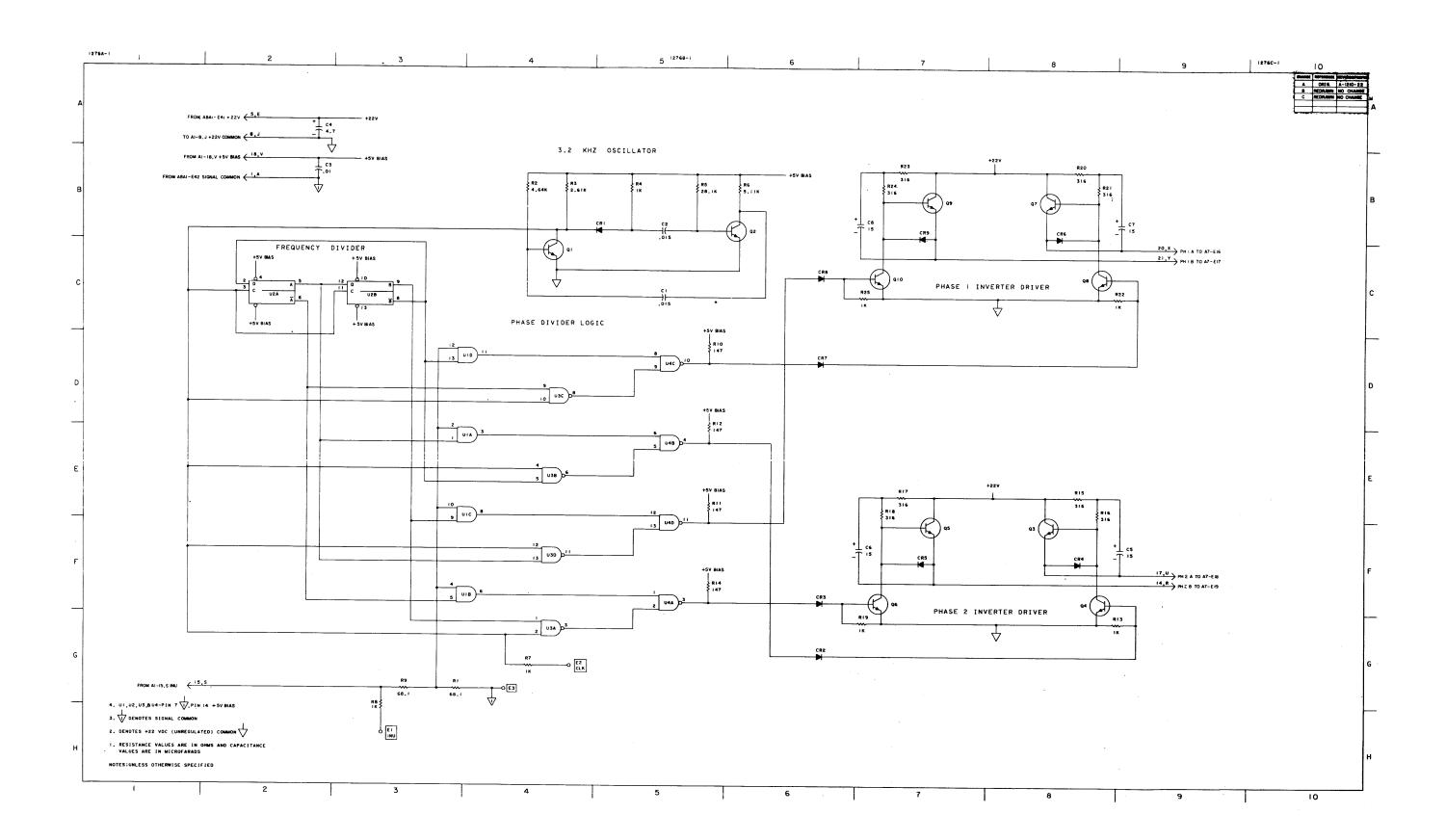
ALL CAPACITANCE IN MICROFARADS

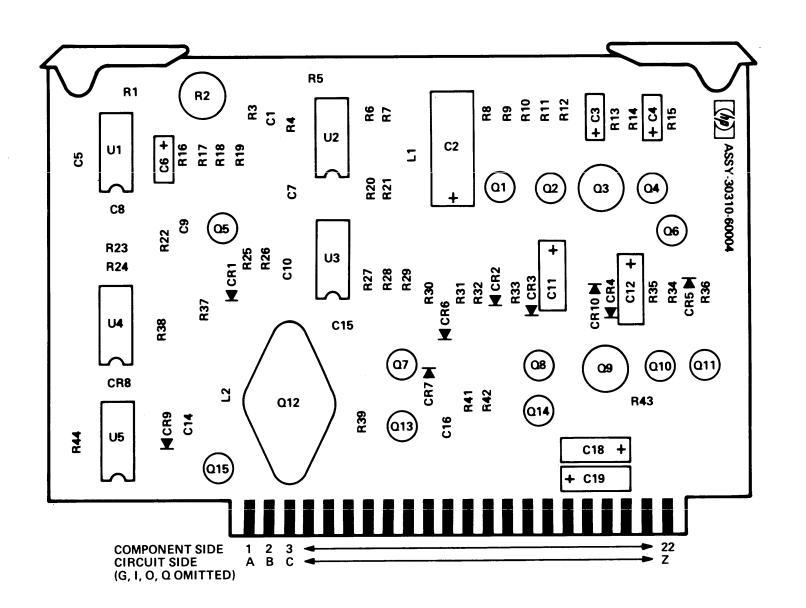
ALL DIODES # 1901-0083

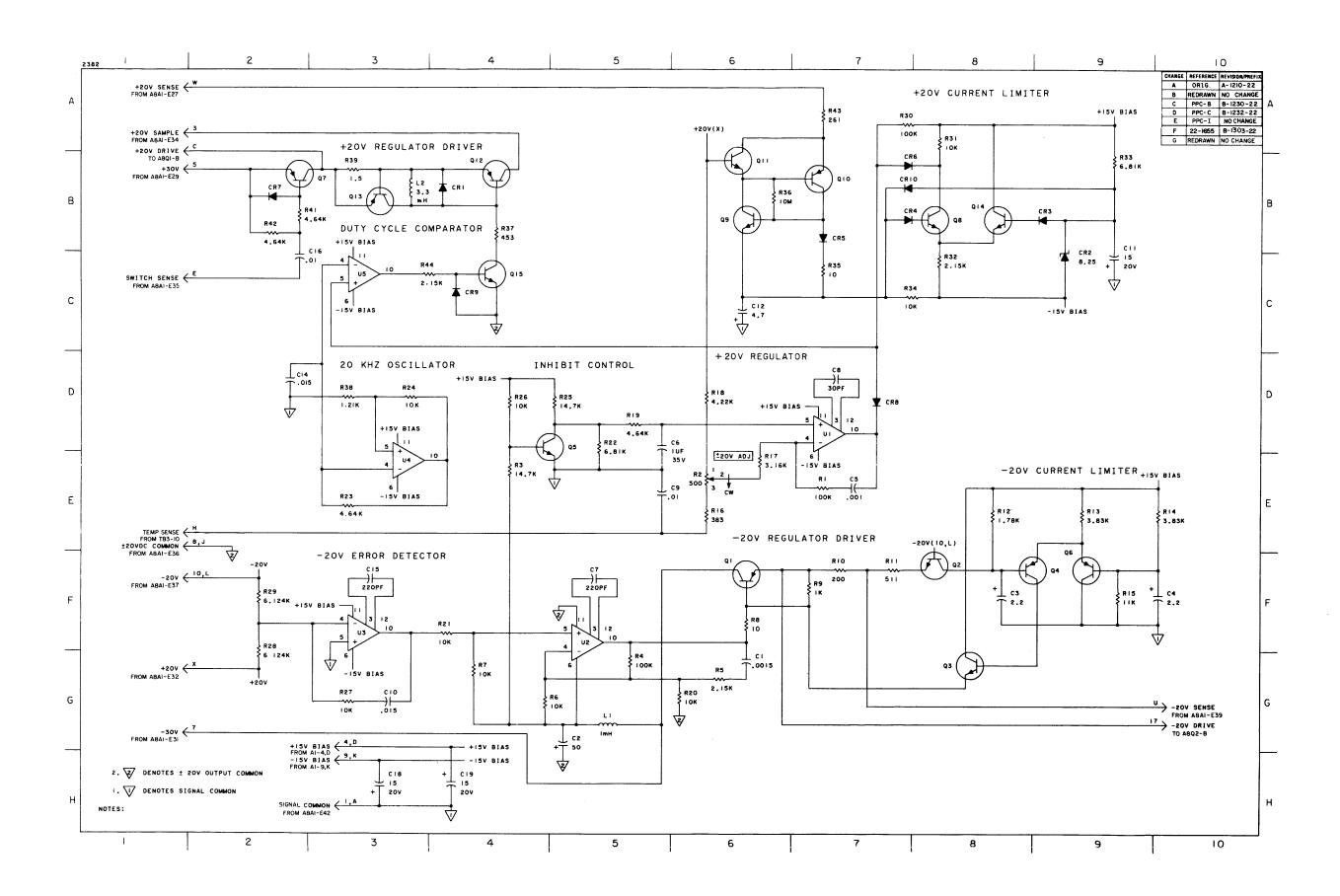
ALL IC'S ARE # 1826-

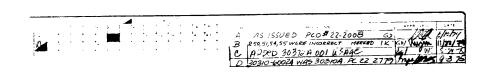


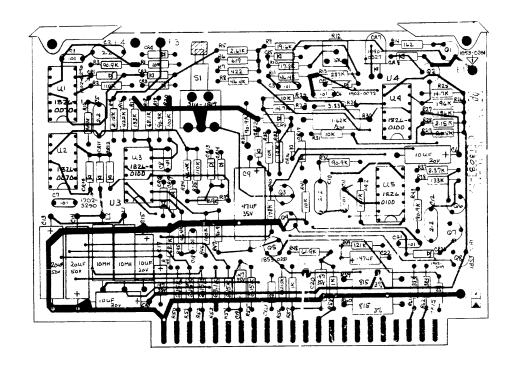




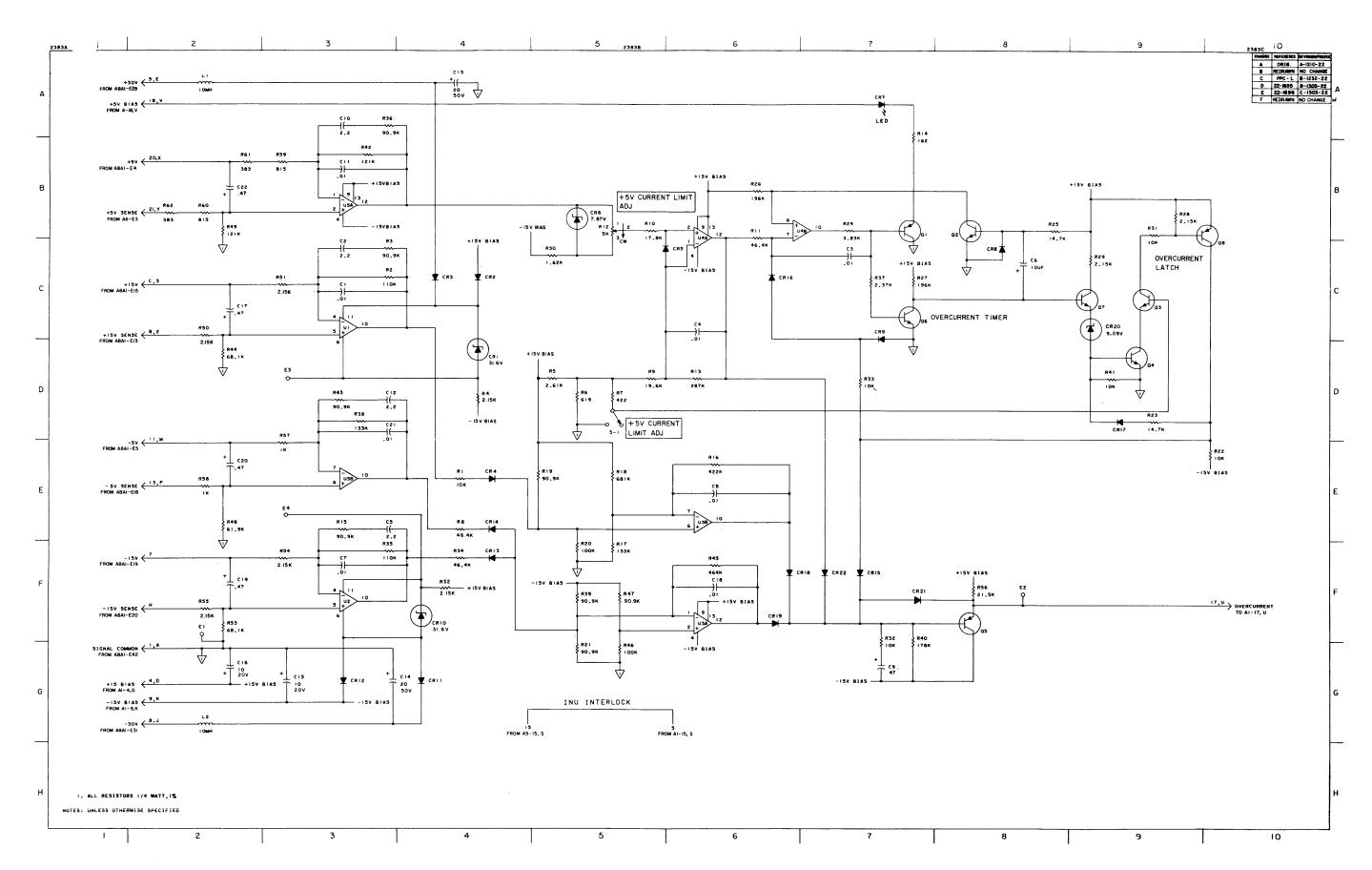


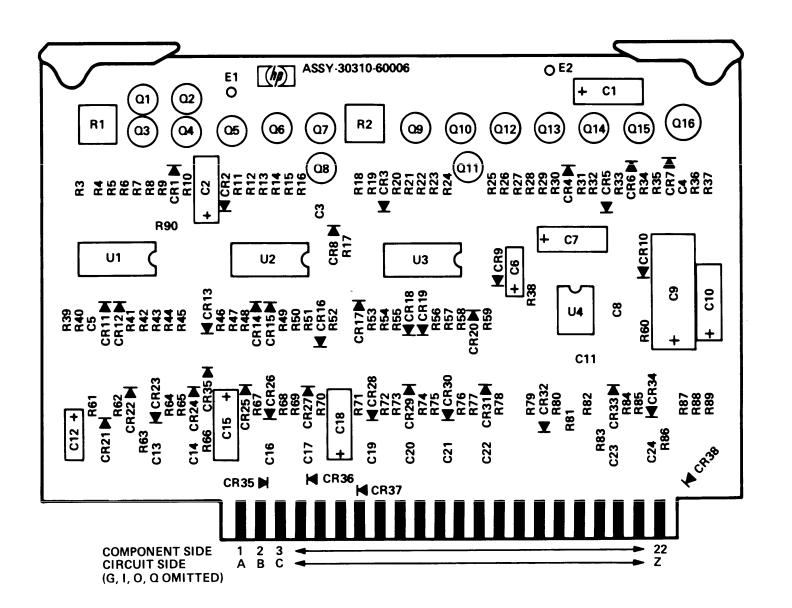


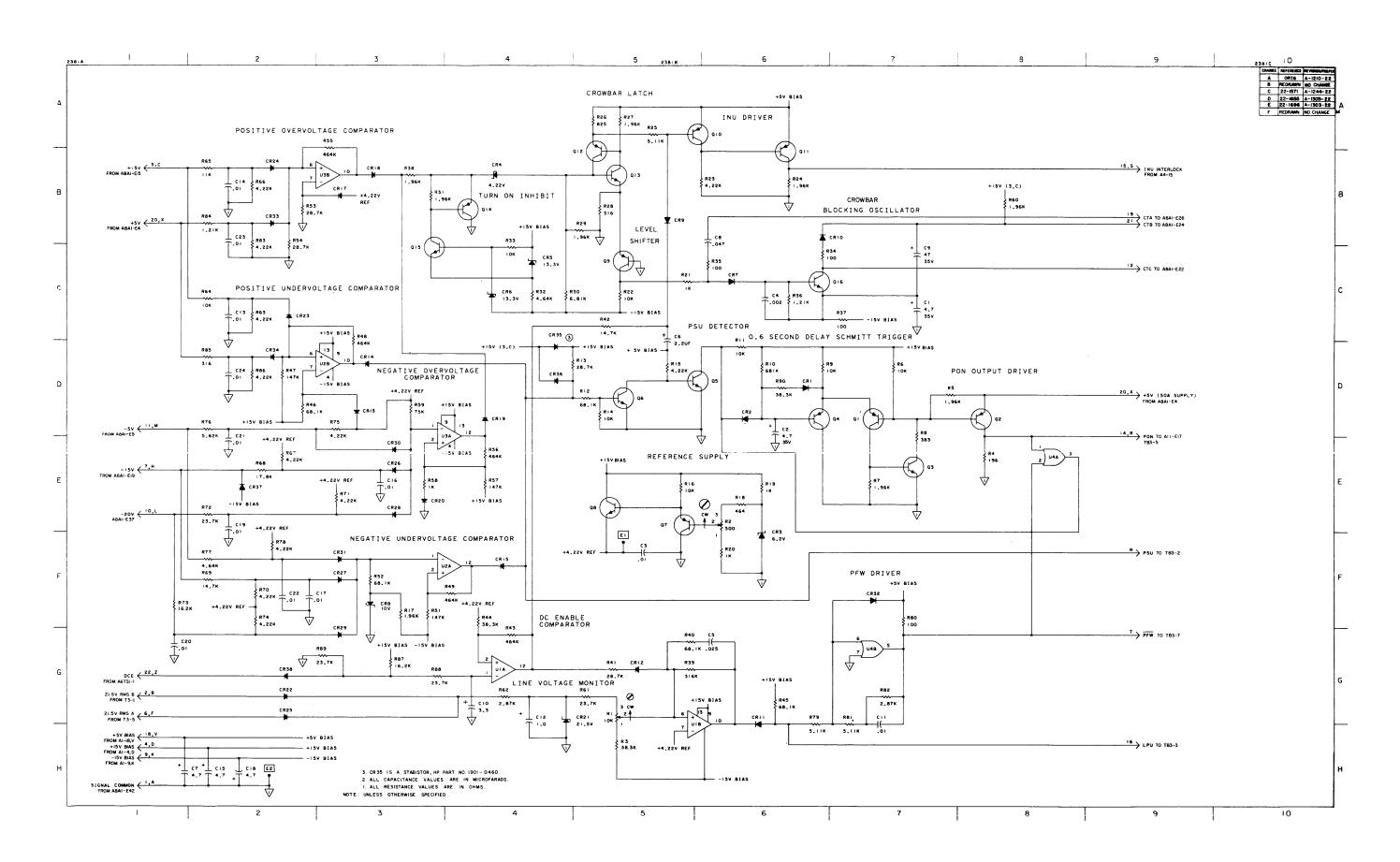


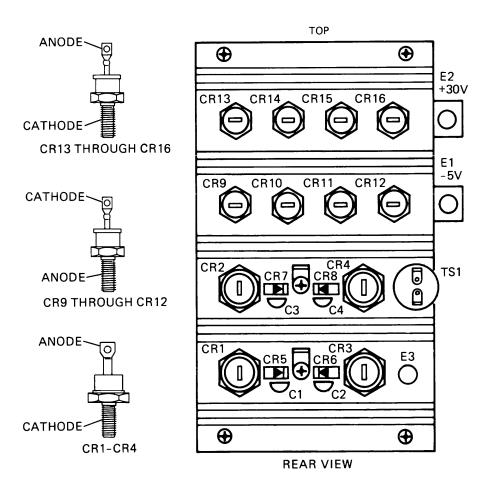


UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IN OHMS
ALL RESISTORS %W 1%MF
ALL CAPACITANCE IN MICROFARADS
ALL CAPACITORS .01UF CERAMIC DISC
ALL DIODES 1901-0033
ALL TRANSISTORS 1854-0477





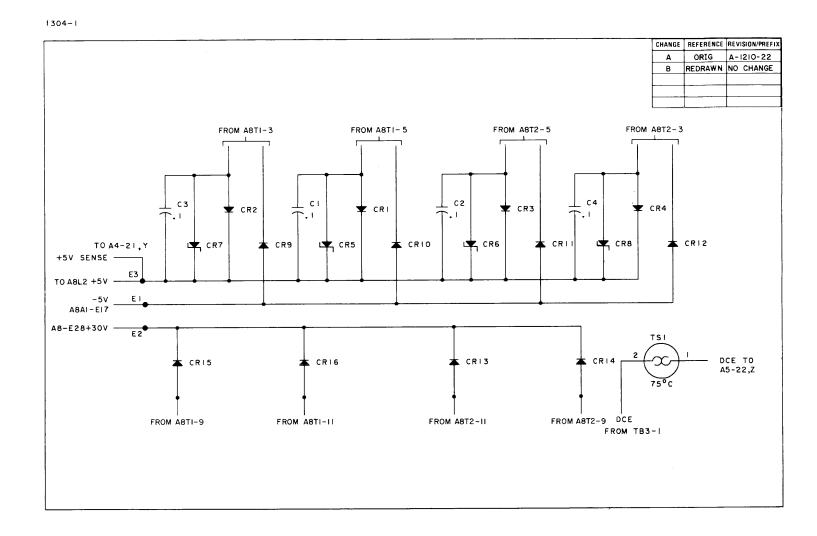




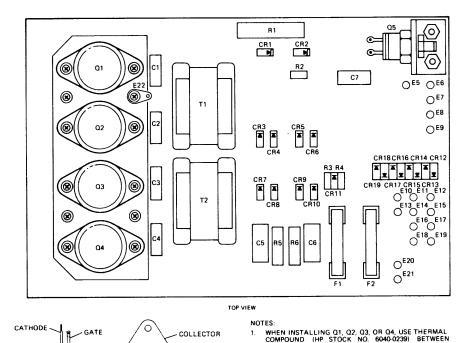
7011-26

NOTES:

- 1. **CAUTION**. HEAT SINK IS +5V WITH RESPECT TO POWER SUPPLY CHASSIS.
- 2. WHEN INSTALLING DIODES IN THIS ASSEMBLY, USE THERMAL COMPOUND (HP STOCK NO. 6040-0239) ON BOTH SIDES OF INSULATING WASHERS OR ON METAL WASHER AND DIODE MOUNTING SURFACE.
- 3. TIGHTEN MOUNTING NUTS FOR CR1 THROUGH CR4 TO 30 IN.-LBS (0.35 kg-m).
- TIGHTEN MOUNTING NUTS FOR CR9 THROUGH CR16 TO 15 IN.- LBS (0.17 kg-m).
- 5. REFERENCE DESIGNATION PREFIX IS A6.



32421A ONLY A6 5V/30V Rectifier Assembly, 30310-60011, Sheet 1 of 1



COLLECTOR

Q1, Q2, Q3, Q4 (PINS FACING VIEWER)

7011-31

WHEN INSTALLING Q1, Q2, Q3, OR Q4, USE THERMAL COMPOUND (HP STOCK NO. 6040-0239) BETWEEN TRANSISTOR AND HEAT SINK.

2. WHEN INSTALLING Q5, TIGHTEN MOUNTING NUT TO 15 IN .- LBS (0.17 kg·m).

3. REFERENCE DESIGNATION PREFIX IS A7.

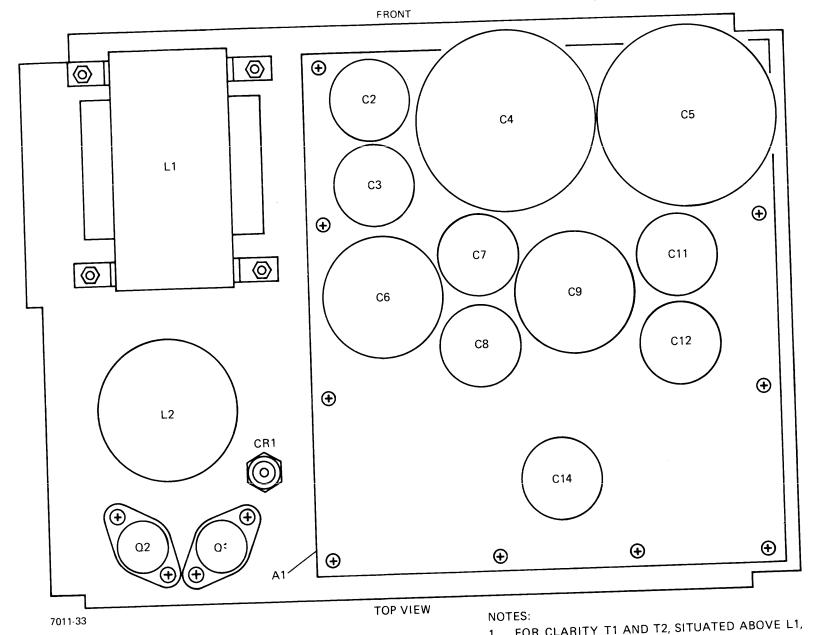
1302-1

NOTE: UNLESS OTHERWISE SPECIFIED

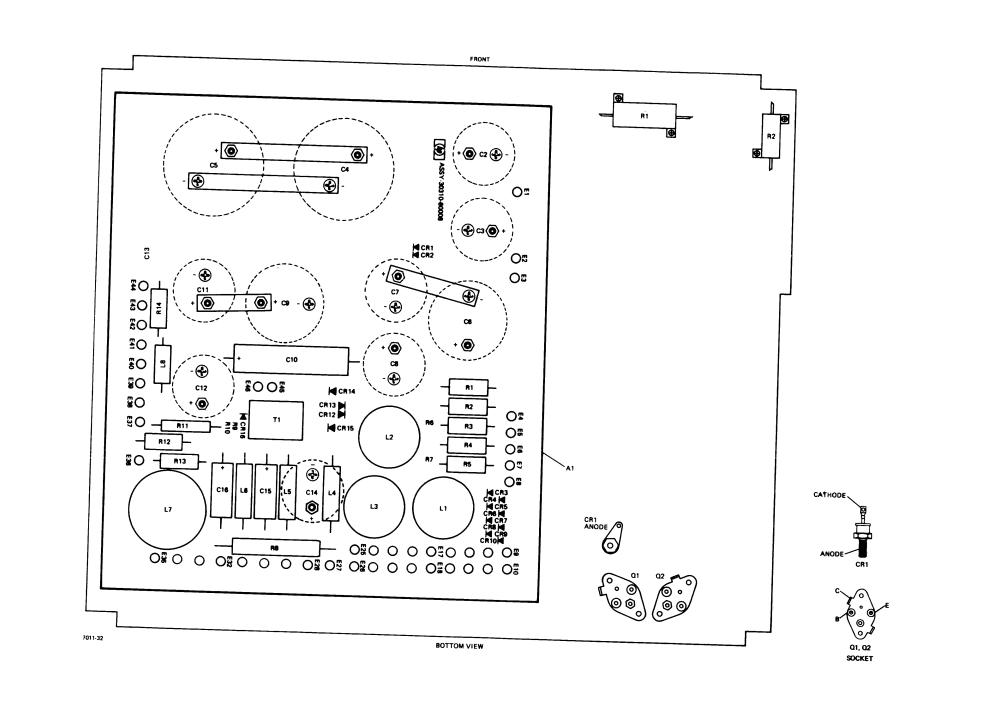
E15 - E10 E17 - E16 - E19 - E18 E 6 C1 7.47 50V **★** CR8 LOOK -30V RECTIFIERS HEAT SINK 3.0A E5 E12 CR13 E CR4 CR14 FROM ASTI-9 CR15 CRIG EII FROM A8T2-9 CR17 A CR6 CRIB E13 ____ c3 ↑.47 50V ★ CR5 CRIS TO A8T2-I E20 A CRIO 100K 1/2W C4 7.47 50V E7 CR2 CRI E9 42.2 42.2 2,25W 75V 75V + C7 R3 FROM A8AI C4(-) A8AI-E46 I. RESISTANCE VALUES ARE IN OHMS ±1%, 4 W.

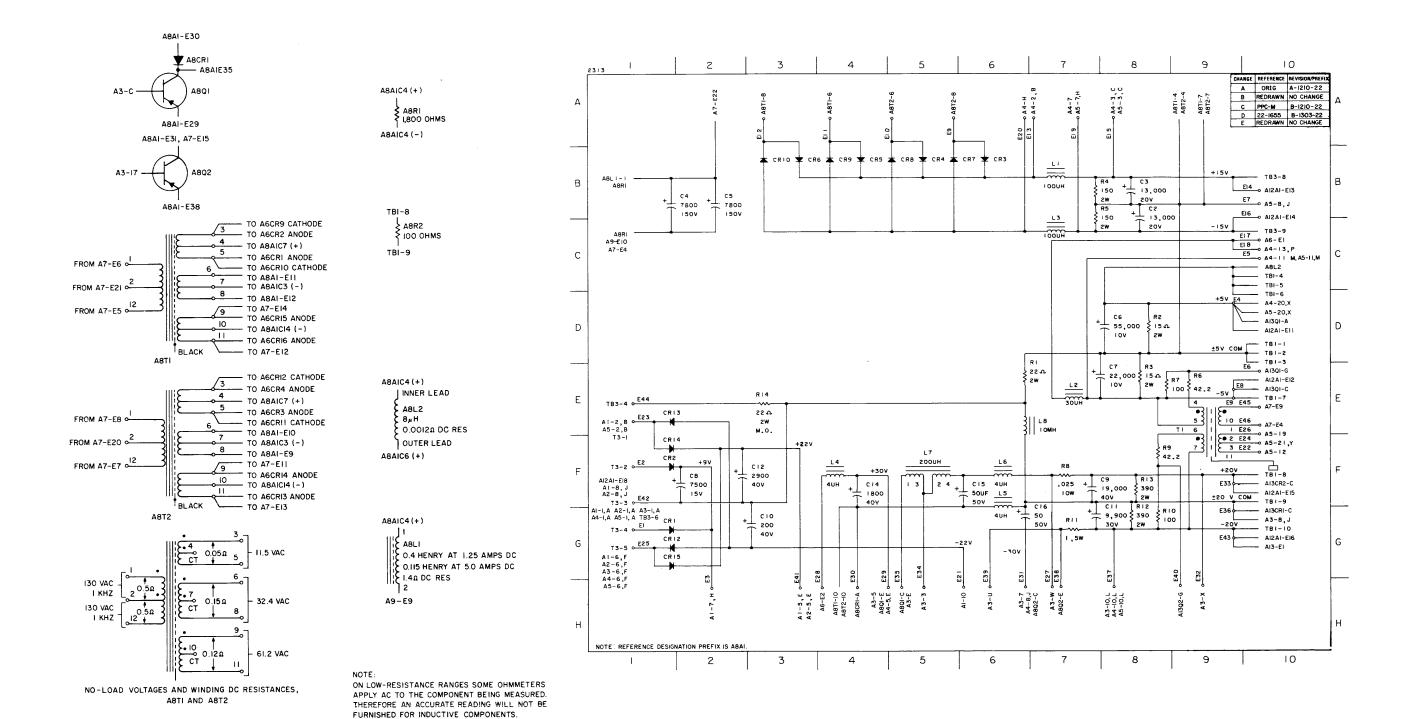
32421A ONLY A7 Inverter PCA, 30310-60007, Sheet 1 of 1

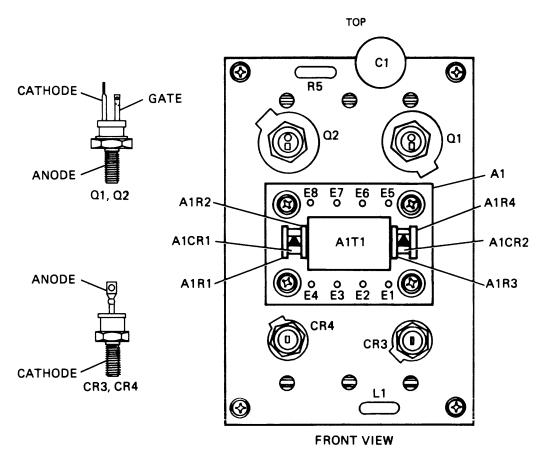
CHANGE REFERENCE REVISION/PREFIX
A ORIG A-1210-22
B REDRAWN NO CHANGE
C 22-1614 B-1210-22 D REDRAWN NO CHANGE



- 1. FOR CLARITY T1 AND T2, SITUATED ABOVE L1, ARE NOT SHOWN.
- WHEN INSTALLING Q1 OR Q2 IN THE TRANSISTOR SOCKET, USE THERMAL COMPOUND (HP STOCK NO. 6040-0239) ON BOTH SIDES OF INSULATING
- TIGHTEN MOUNTING NUT FOR CR1 TO 15 IN.-LBS
- COMPONENTS MAY VARY SLIGHTLY FROM LOCA-TIONS SHOWN.
- REFERENCE DESIGNATION PREFIX IS A8.



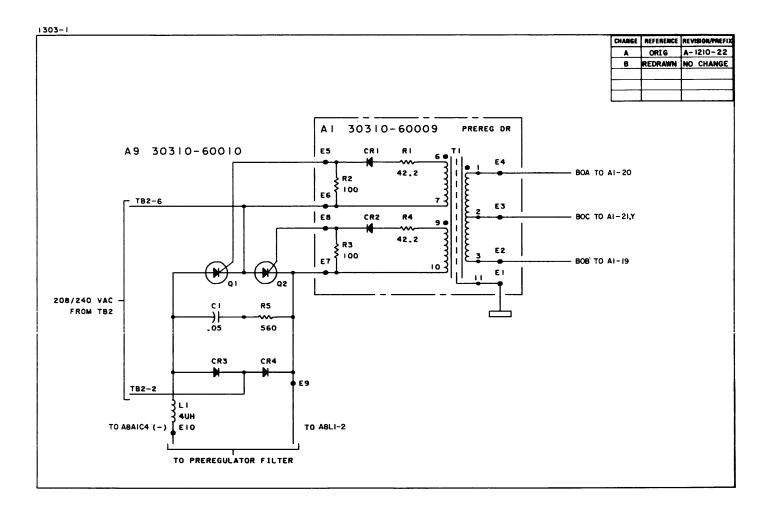


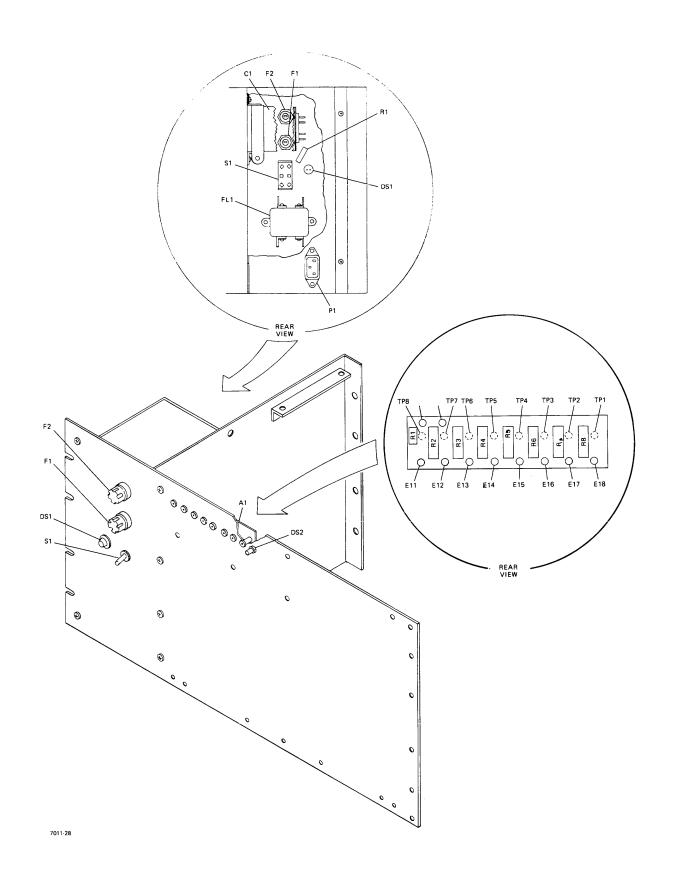


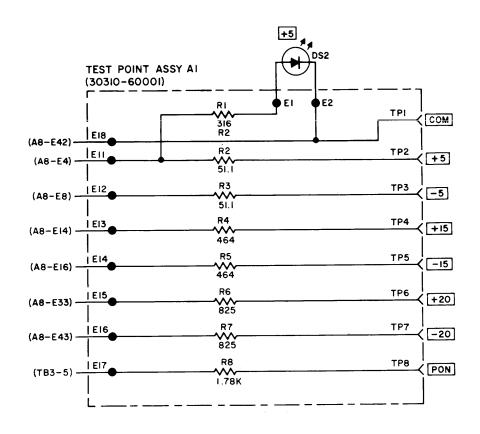
NOTES:

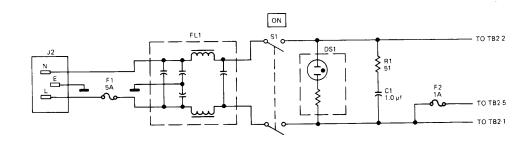
- 1. WHEN INSTALLING SEMICONDUCTOR DEVICES IN THIS ASSEMBLY, USE THERMAL COMPOUND (HP STOCK NO. 6040-0239) ON BOTH SIDES OF INSULATING WASHERS.
- 2. TIGHTEN ALL SEMICONDUCTOR MOUNTING NUTS TO 15 IN.- LBS (0.17 kg-m).
- 3. WHEN INSTALLING PLASTIC SCREWS USE THREAD SEALANT (HP STOCK NO. 0470-0013). DO NOT TIGHTEN EXCESSIVELY.
- 4. REFERENCE DESIGNATION PREFIX IS A9.

7011-30



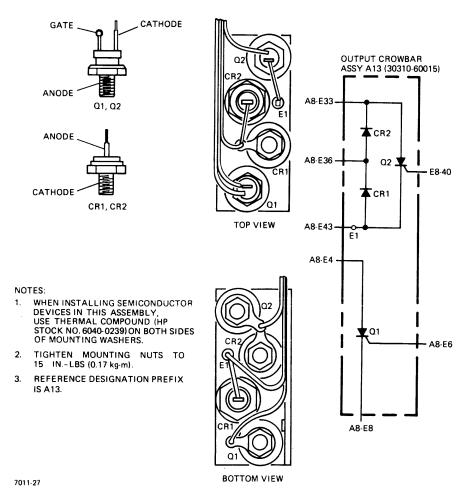




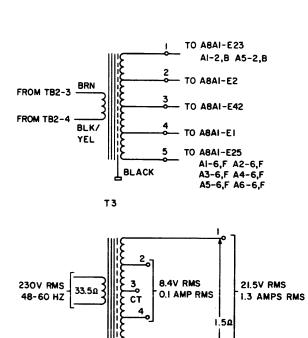


NOTES:
I. RESISTANCE VALUES
ARE IN OHMS.
2. REFERENCE DESIGNATION
PREFIX IS AI2.

32421A ONLY Al2 Front Panel Assembly, 30310-60013, Sheet 1 of 1





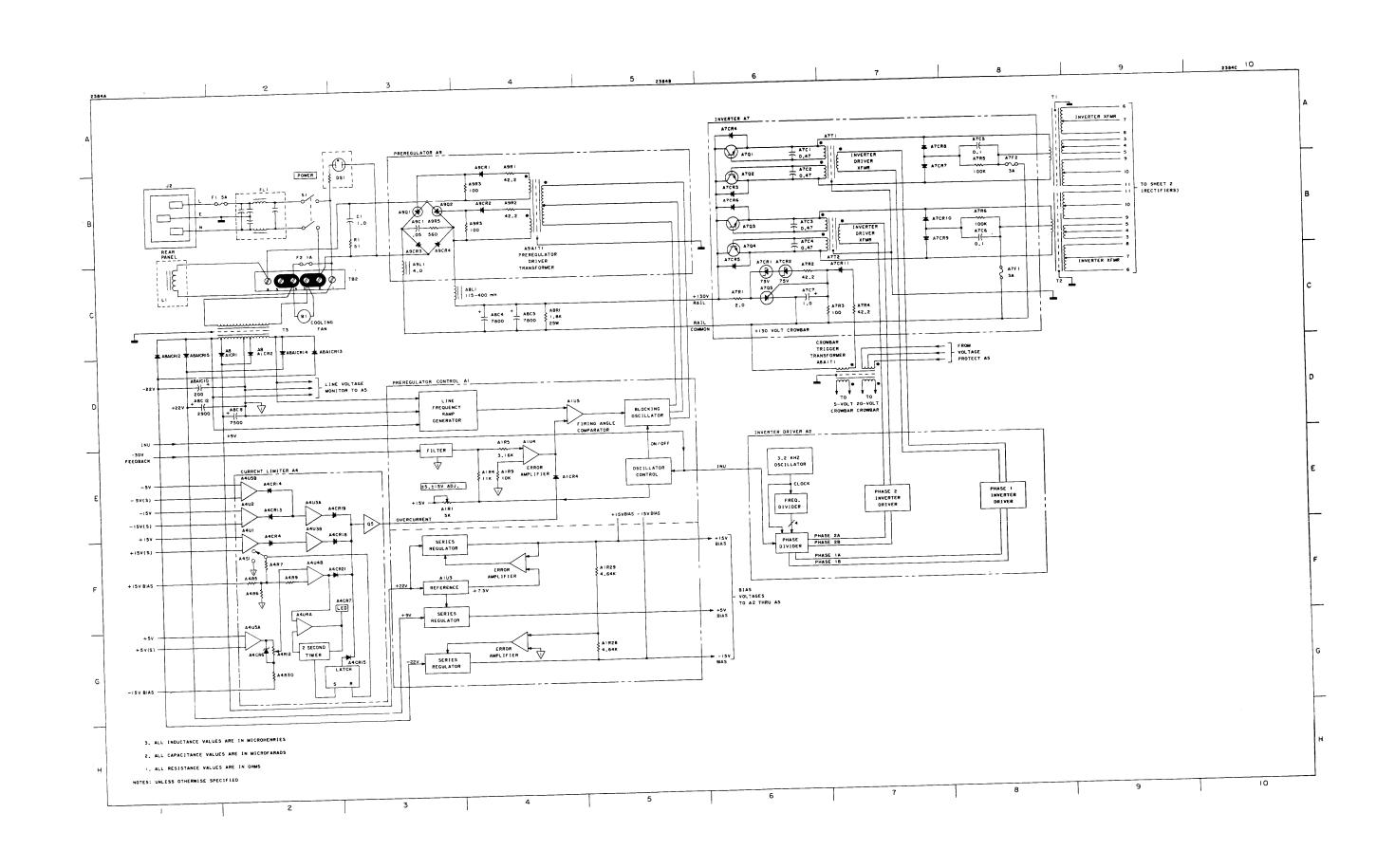


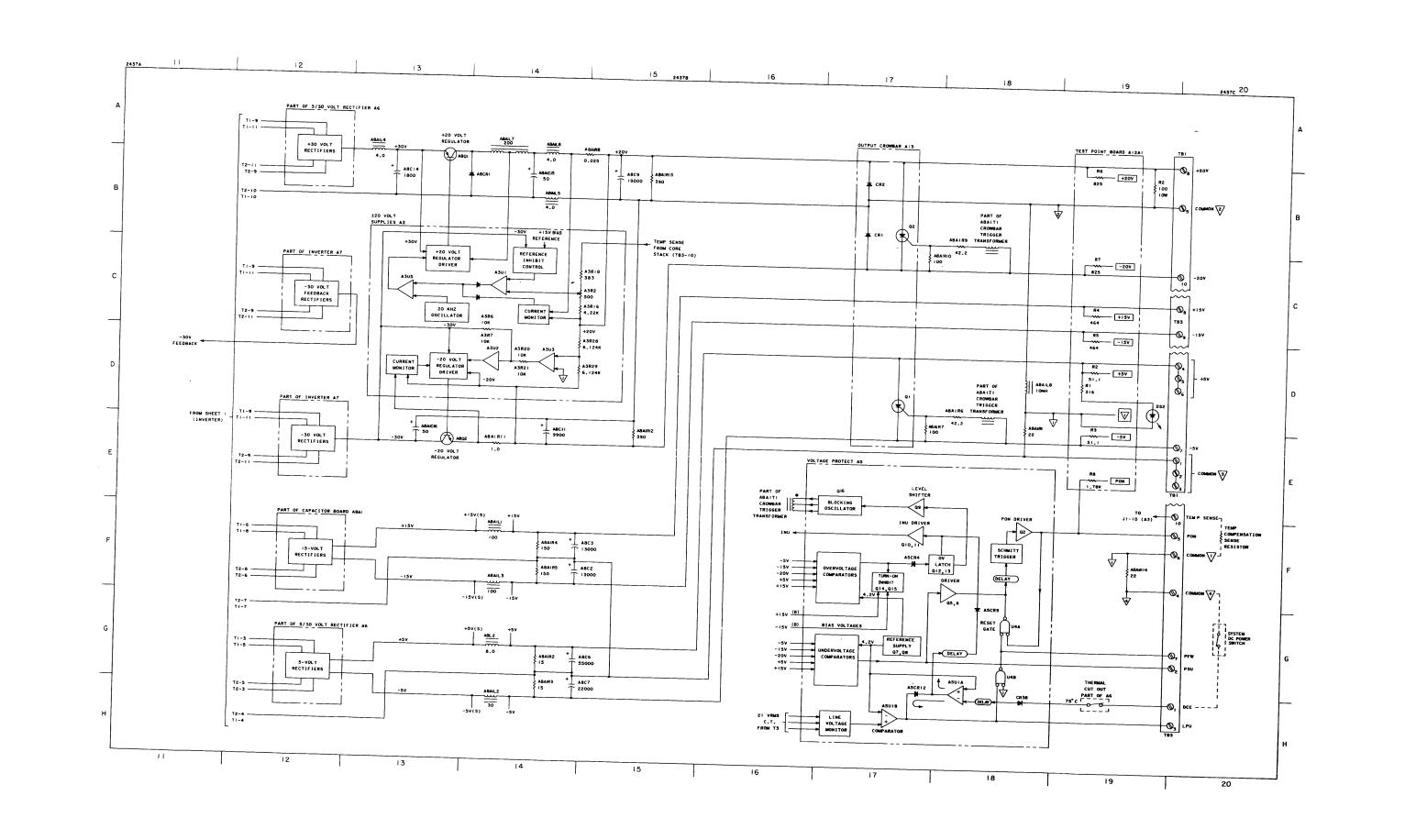
NO-LOAD VOLTAGES AND WINDING DC RESISTANCES, T3

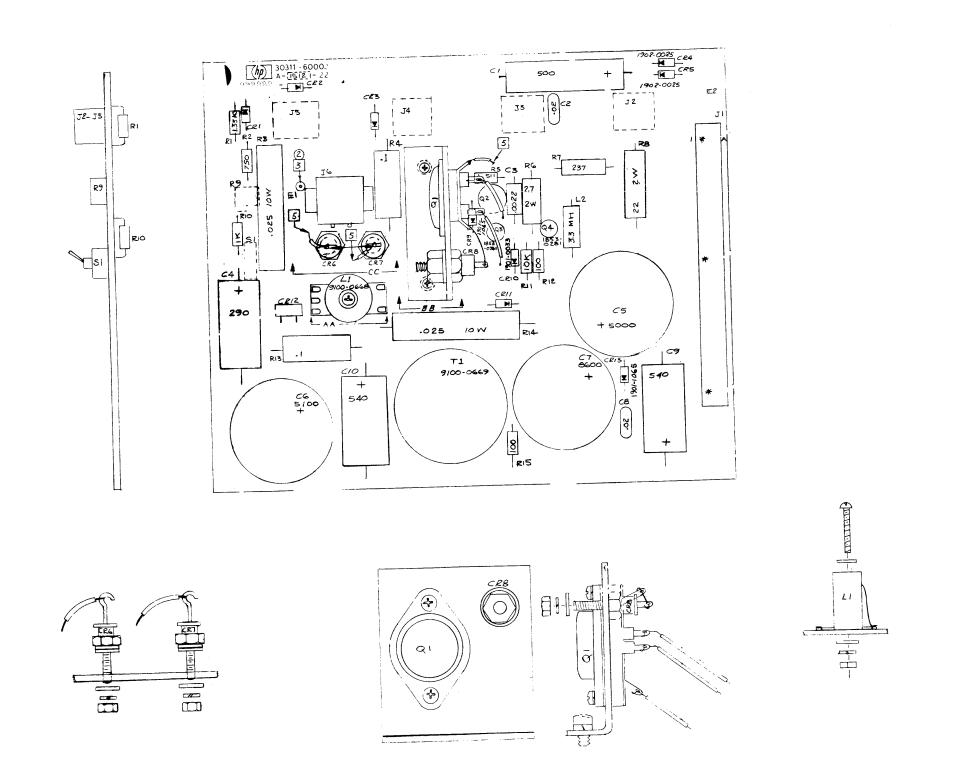
NOTE:
ON LOW-RESISTANCE RANGES SOME OHMMETERS APPLY
AC TO THE COMPONENT BEING MEASURED. THEREFORE
AN ACCURATE READING WILL NOT BE FURNISHED FOR
INDUCTIVE COMPONENTS.

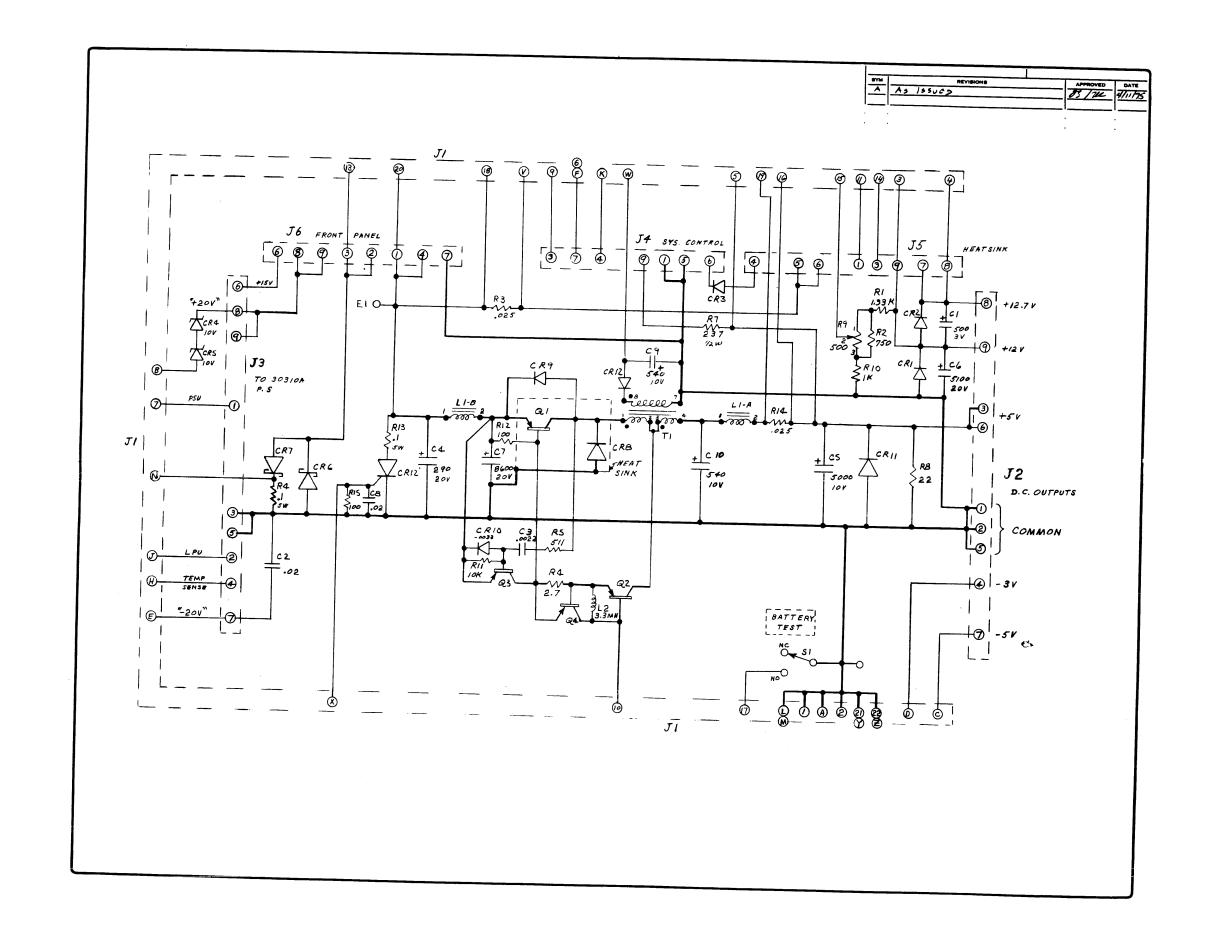
FAN B1, CHOKE L1, TRANSFORMER T3

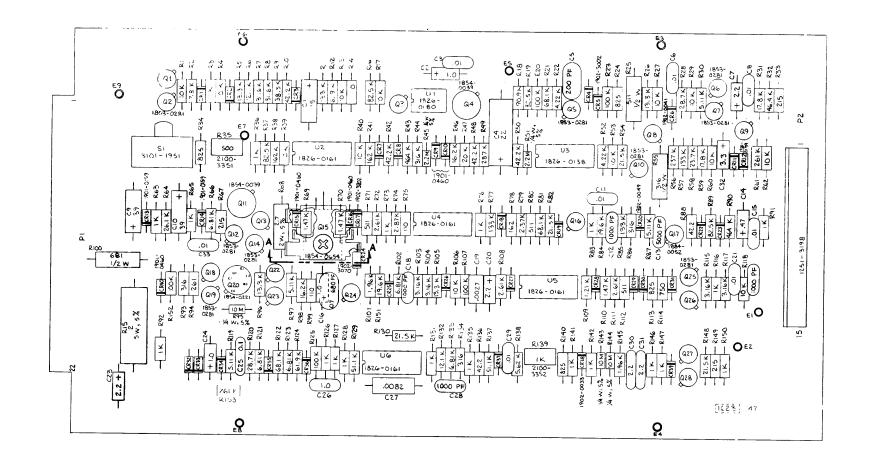
32421A ONLY Al3 Output Crowbar Assembly, 30310-60015, Sheet 1 of 1





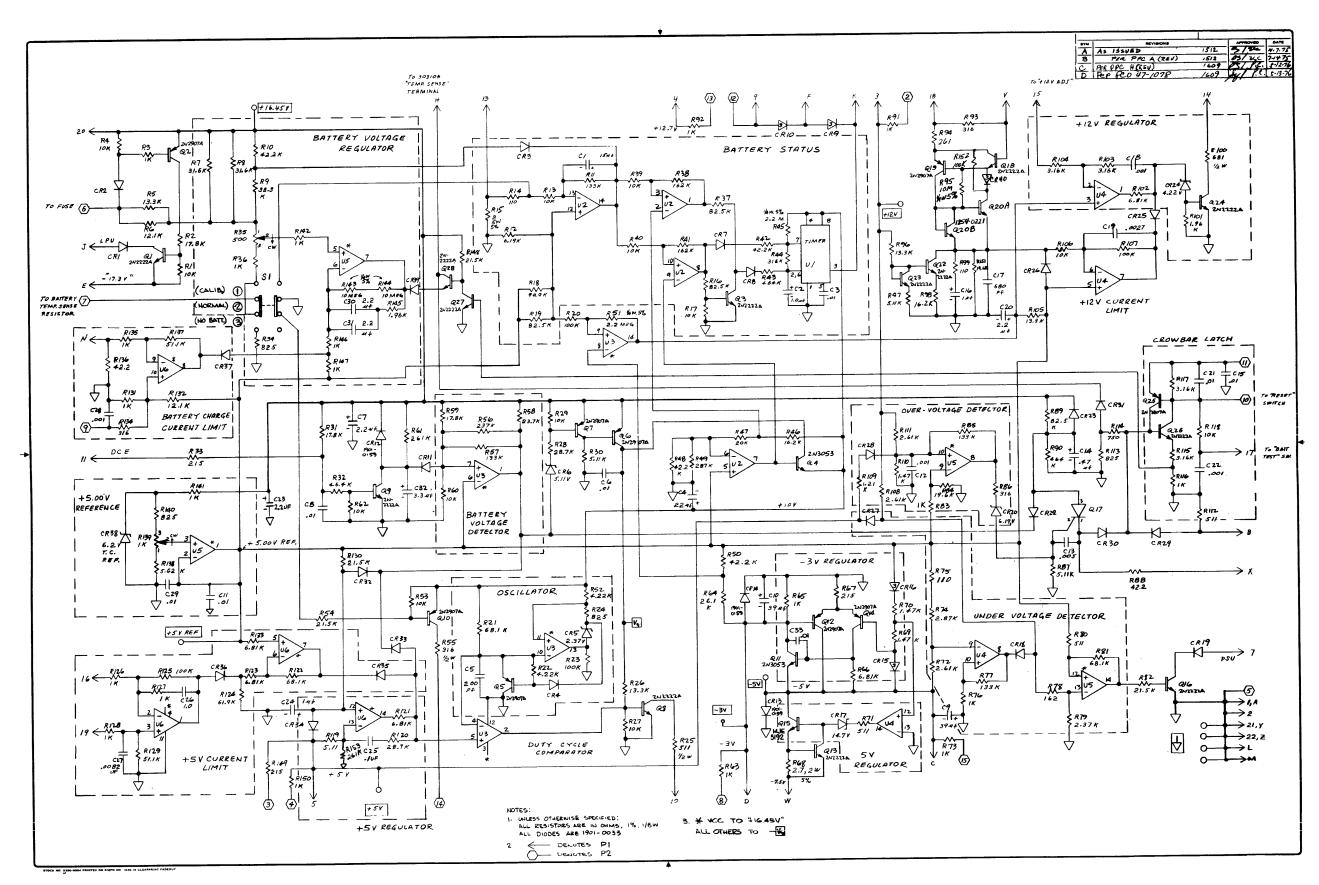


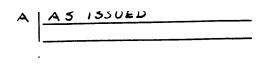


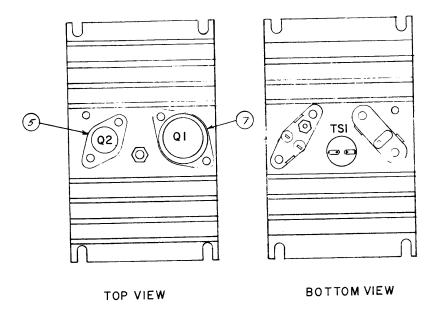


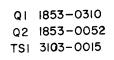
NOTES:

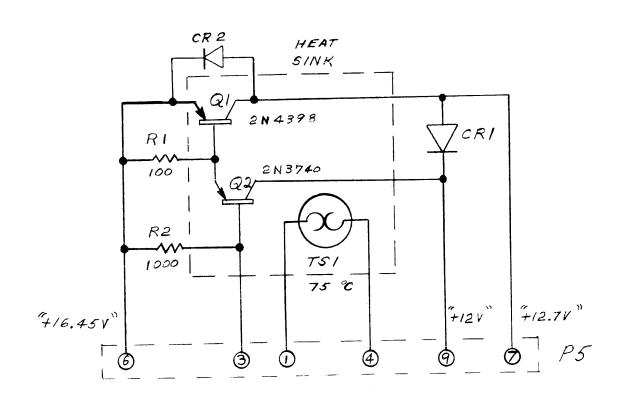
1. UNITES CTHERWISE SPECIFIED:
ALL RESISTORS ARE IN OHMS 11%, 8 w
ALL CAPACTORS ARE IN MICROFARADS
ALL TRANSISTORS ARE 1854-0477
ALL DIODES ARE 1901-0033

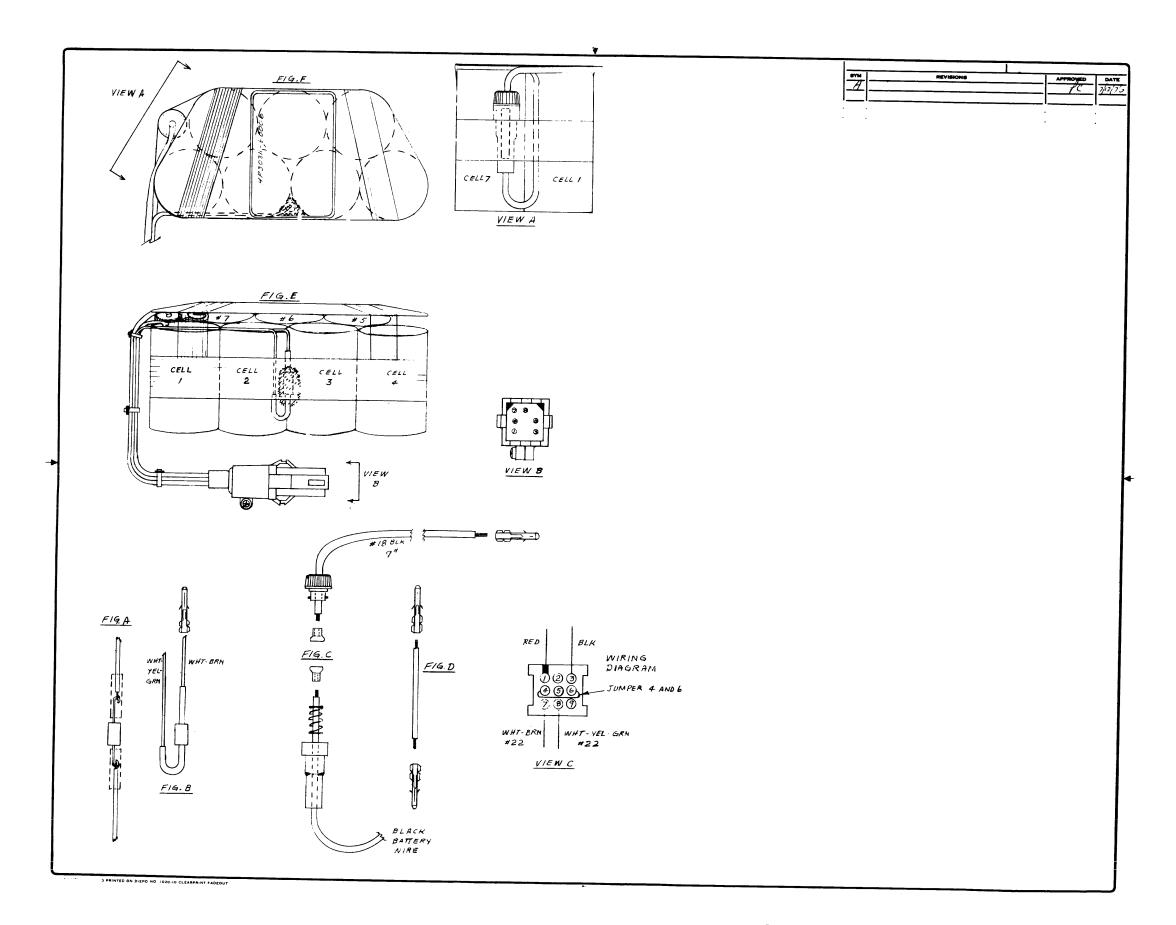


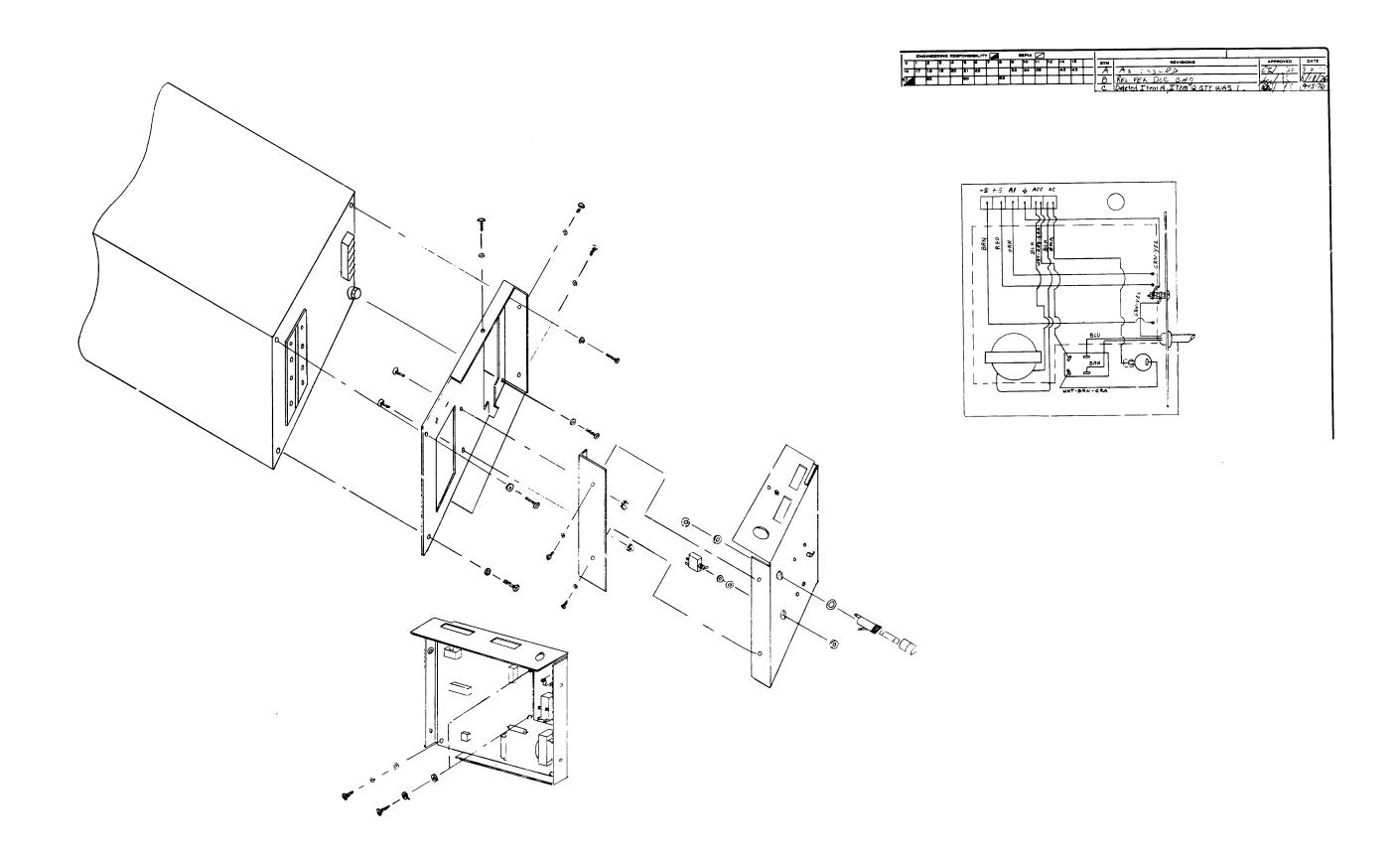


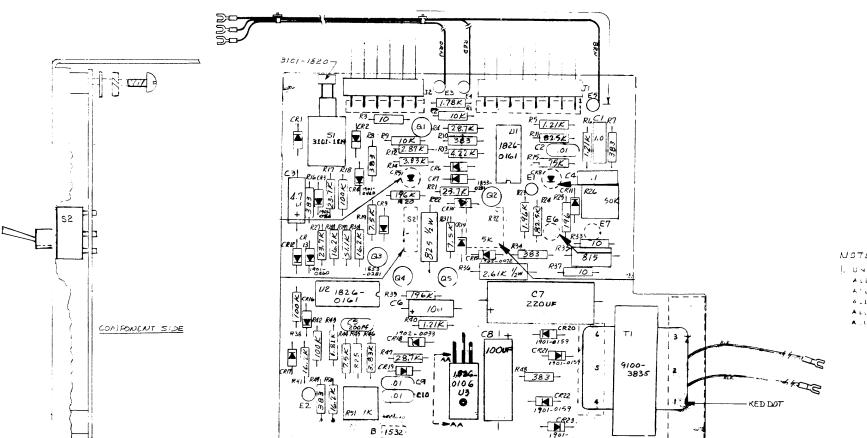










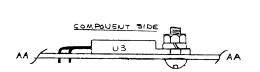


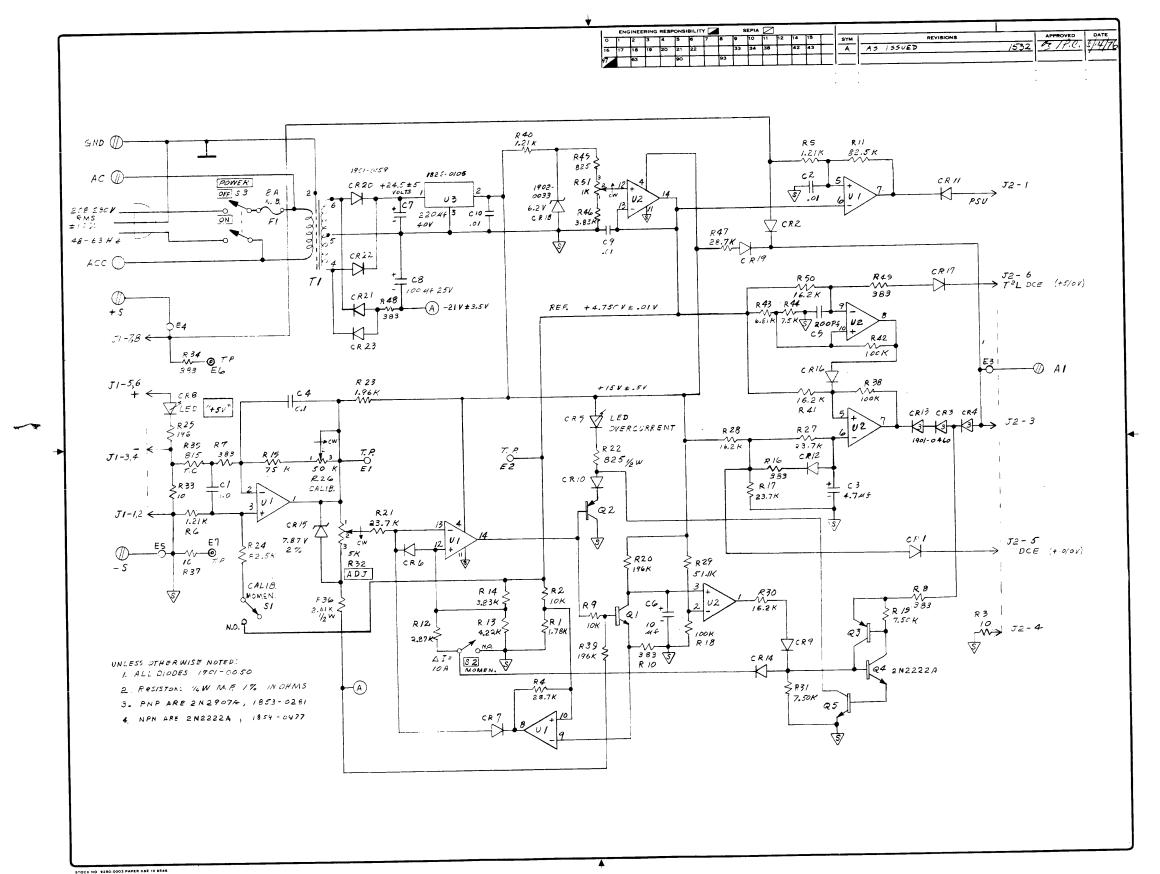
A AS ISSUED

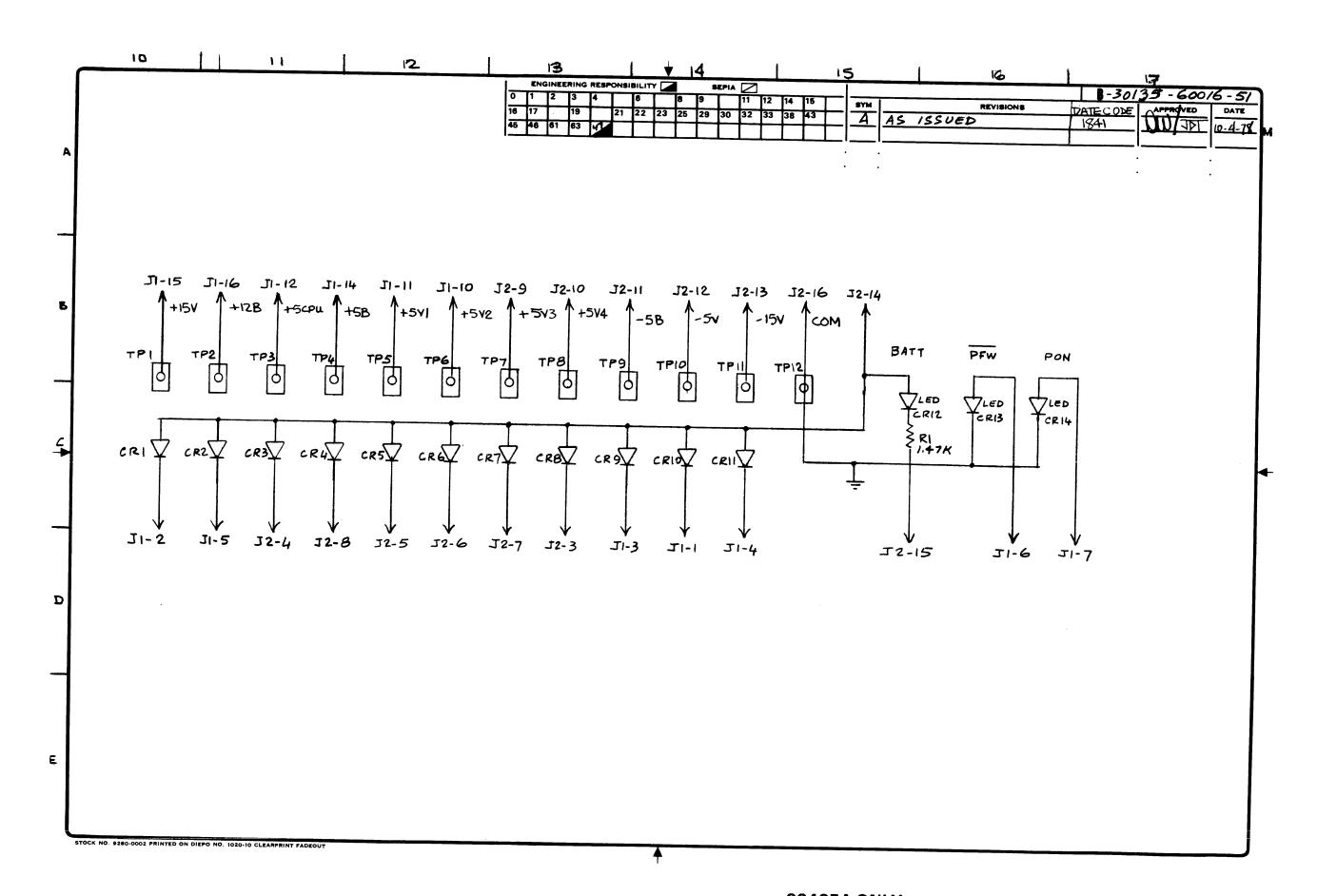
MOTES:

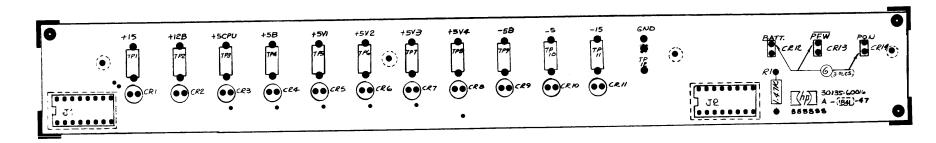
LUNLESS OTHERWISE SPECIFIED: ALL RESISTANCE IN OHMS ALL RESISTORS 1/8W, /

AL CAPACITANCE INMICROFARADS AL TRANSISTORS - 1854-0477 AL CIODES - 1901-0050



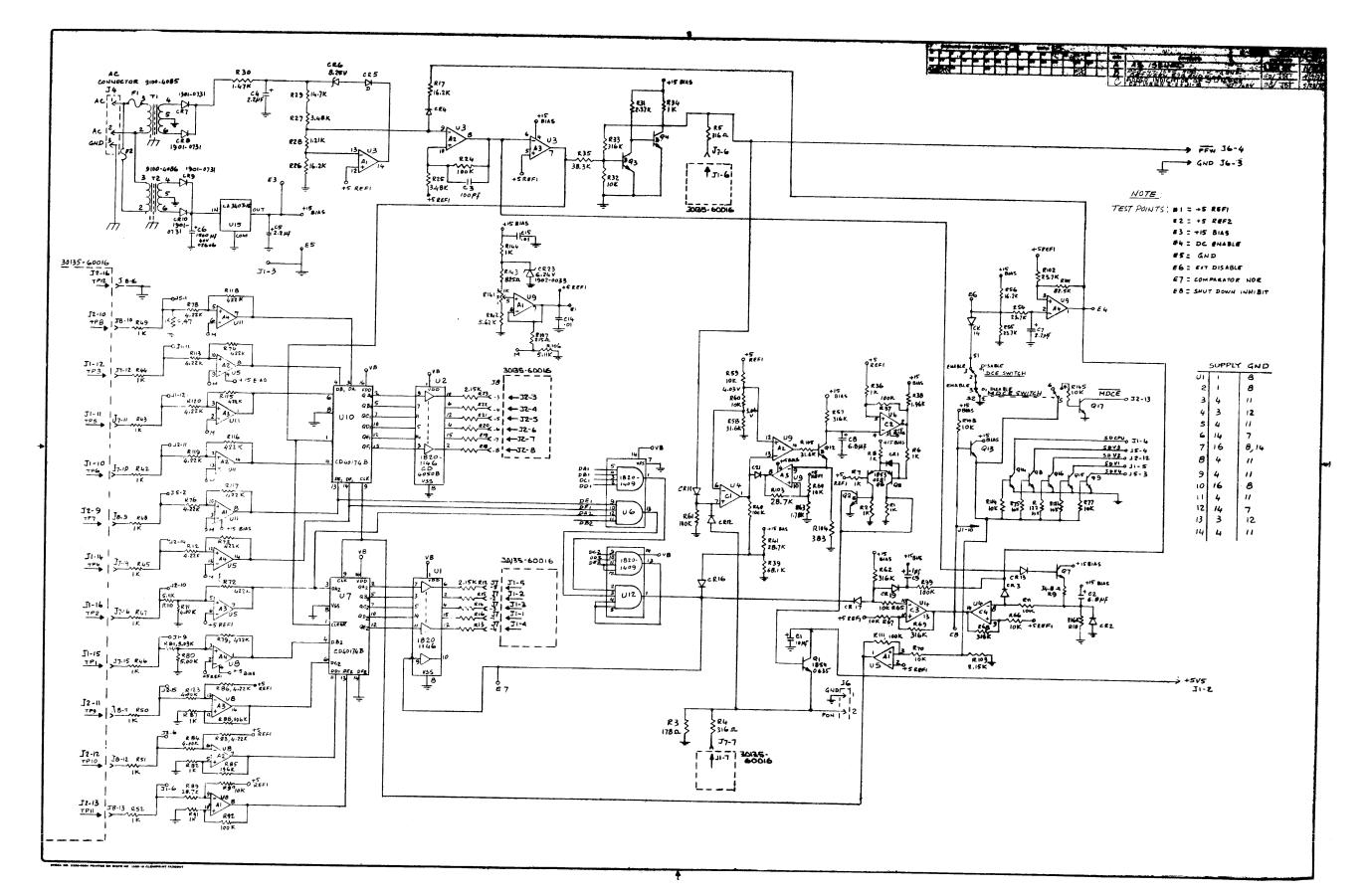




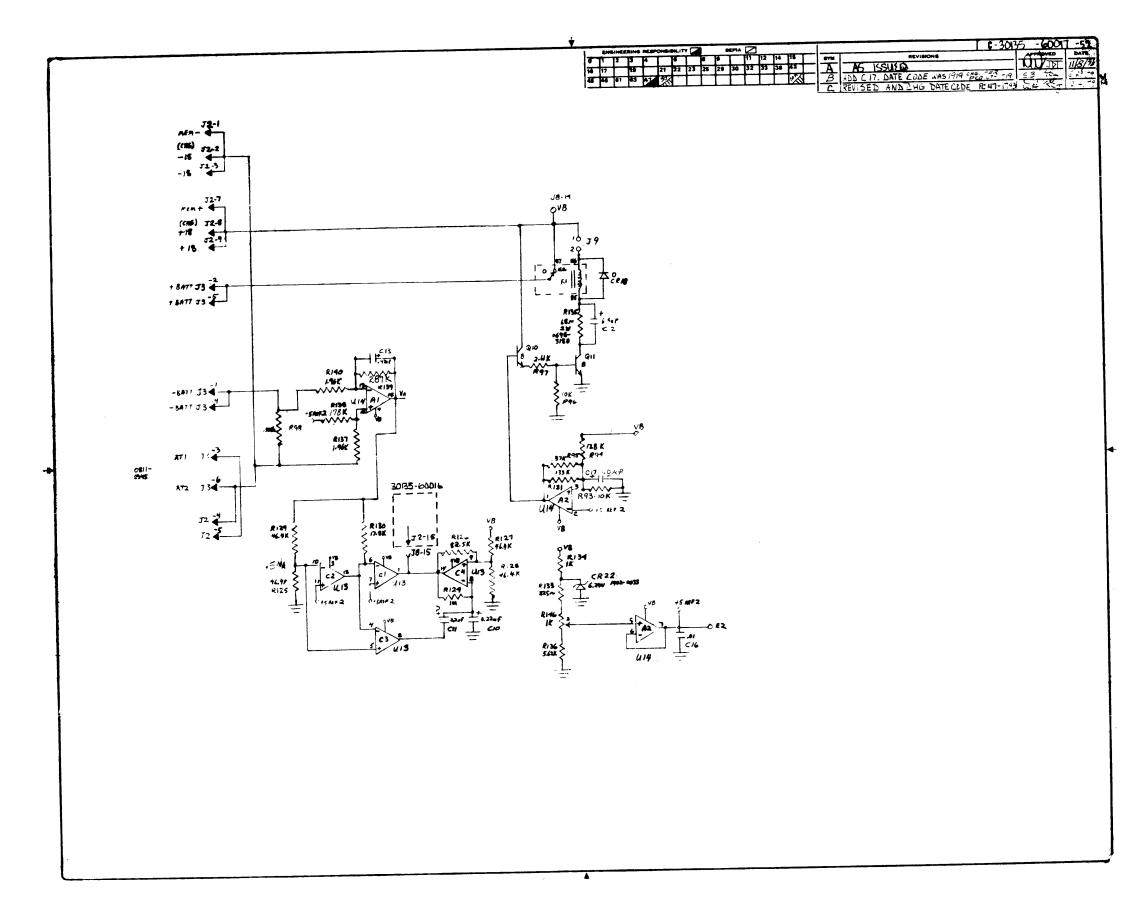


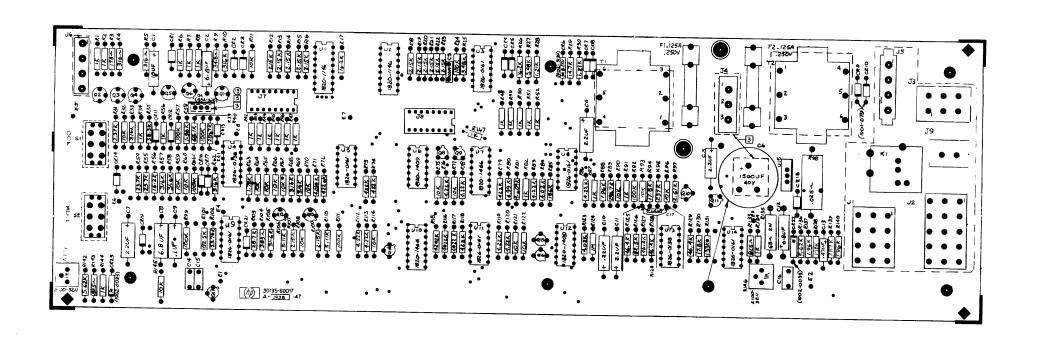
NOTES

I. UNLESS OTHERWISE SPECIFIED;
ALL RESISTANCE INGHMS '18W 170.
ALL LED'S ARE 1790-0486
ALL TEST POINTS ARE 1251-1375



32435A ONLY DC Power Control PC, 30135-60017, Sheet 1 of 3





NOTES:

I. UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTANCE ARE 78 W 190
ALL DIODES ARE 1801-1098
ALL TRANSISTORS ARE 1866-003